BDC based burstmode receiver in PON systems

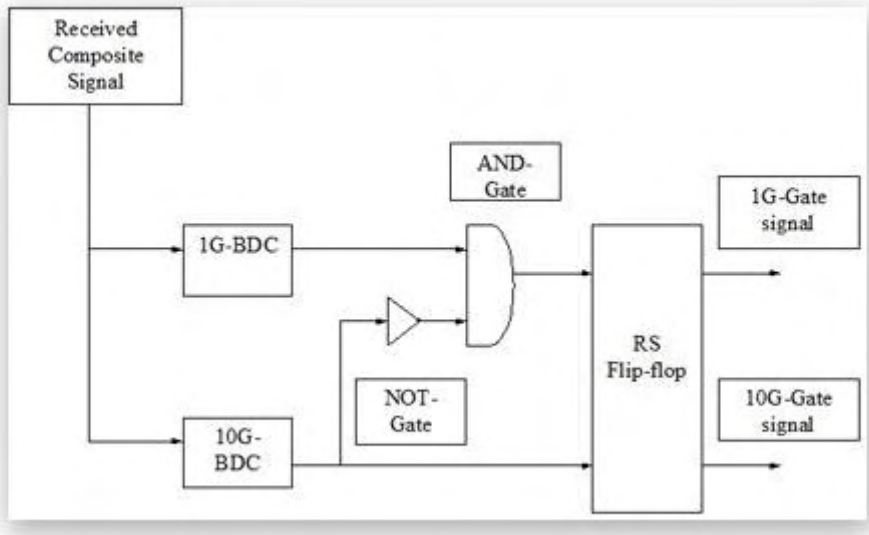
Tool Used: OptSim

This example demonstrates the functioning of an advanced Bitrate Discrimination Circuit (BDC) based dual-rate burstmode receiver.

Bitrate Discrimination Circuit (BDC) based burstmode receiver using SPICE cosimulation in OptSim. This example is based on the Burst-mode receiver model reported in the paper in [1] ("Burst-mode Bit-rate Discrimination Circuit for 1.25/10.3-Gbit/s Dual-rate PON Systems" by Kazutaka Hara, Shunji Kimura, Hirotaka Nakamura, Naoto Yoshimoto, and Kiyomi Kumozaki). It basically demonstrates the functioning of an advanced Bitrate Discrimination Circuit (BDC) based dual-rate burstmode receiver that can be used to detect a time-division multiplexed composite burstmode signal with dual bitrates and separate out the data bursts of each bitrate. A data burst is typically made of a preamble, which consists of a known sequence of data bits followed by the actual payload. The BDC-based burstmode receiver makes use of the unique preamble sequence sent at the start of each burst signal to implement a logic that generates a gate signal for transmitting that particular burst through.

The main block in this receiver is the Burstmode-Bitrate Discrimination Circuit (B-BDC), which is made up of two BDC circuits, one for each bitrate. The block diagram of the B-BDC circuit is shown below:

The figure below shows the block diagram of Burstmode-Bitrate Discrimination Circuit (B-BDC) unit [1]



Trigger pulses generated by the BDC components by using the preamble sequence of each burst, are converted into corresponding gating signals by an RS flip-flop as shown in the figure. Each BDC component consists mainly of the following three circuits:

1. EX-OR Gate

2. Integrator Circuit and a
3. Comparator Circuit

The preamble sequences used for each of the bitrates in this project are:

- Alternating sequence ("010101...") for the bursts with bitrate of 10.3Gbps
- Cyclic sequence ("01100110...") for the bursts with bitrate of 1.25Gbps

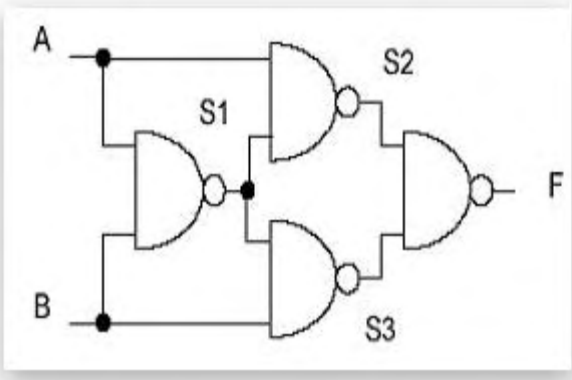
So the BDC components in this project use an Ex-OR logic gate along with a delay of 97.08ps and 1.6ns (corresponding to 1-bit delay and 2-bit delay) for the data bursts of bitrates 10.3Gbps and 1.25Gbps respectively.

In OptSim, the BDC-based burstmode receiver can be implemented using the powerful SPICE co-simulation feature available in the sample-mode of OptSim. Separate CCS components have been used to define individual circuits that make up the BDC and flip-flop units for easy accessibility if the user wants to make design changes. Using individual CCS components also helps in keeping constant track of the signal, thus making it easy to debug the project in case of any issues.

These individual components defined by the SPICE circuit files inside each CCS component are listed below:

Ex-OR Gate: The Ex-OR gate is implemented using 4 NAND-gates.

The figure below depicts the implementation of EX-OR logic using NAND gates:



Each NAND gate in turn is made up of a combination of PMOS and NMOS-based switching elements. To give a better picture on the SPICE circuit files, the circuit file "spice_int_test_XOR_1G.cir" is reproduced below:

```
xnand1      in1     in2     2       nand_gate
xnand2      in1     2       3       nand_gate
xnand3      2       in2     4       nand_gate
xnand4      3       4       out     nand_gate
Rout1       out     0       0.75E6
Cout        out     0       0.0085E1PF
*
************NAND_GATE SUBCKT**********
.Subckt     nand_gate       11      12      5
Mp1         5       11      1       1       P_MO
Mp2         5       12      1       1       P_MO
Mn1         5       12      2       0       N_MO
Mn2         2       11      0       0       N_MO
*RL5        1       5000K
*CL5        0       0.05E-3PF
Vc   1     0     5V
.MODEL P_MO PMOS (LEVEL=1)
.MODEL N_MO NMOS (LEVEL=1)
.Ends nand_gate
*
```

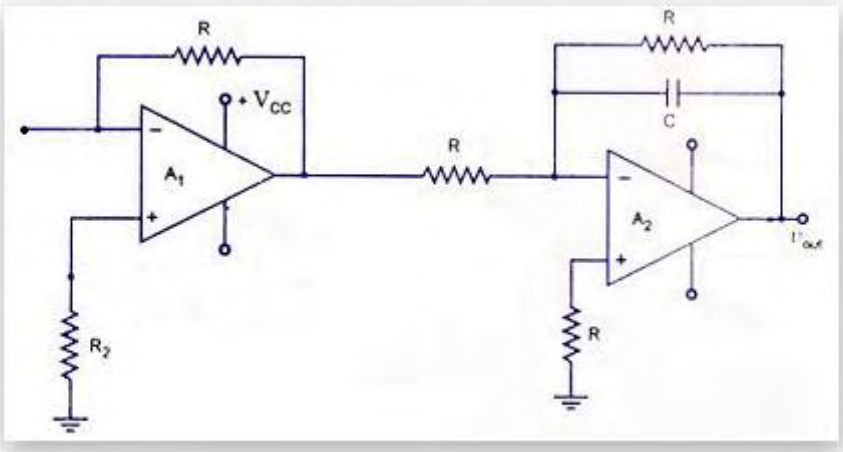
SPICE circuit file "spice_int_test_XOR_1G.cir" for implementing the EX-OR gate

As can be seen, the file uses 4 components of NAND gate, which is defined as a subcircuit below the main circuit. Also, in the definition of the sub-circuit, PMOS and NMOS components have been used, and hence they are declared inside the sub-circuit routine. The values of the output resistor (Rout) and the output capacitor (Cout) have been fine-tuned to adjust the transition time between the two states so that the output appears smooth.

Integrator:

The integrator circuit file actually consists of two cascaded OPAMP circuits -the first OPAMP acts as an inverter to the incoming signal before inputting it to the actual integrator implemented using the second OPAMP circuit.

The figure below depicts the implementation of the integrator circuit using OPAMPS:

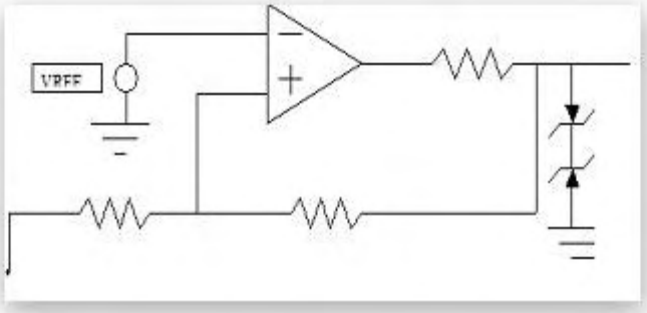


Note here that we have used a feedback resistor in parallel to the capacitor in the integrating OPAMP circuit to make sure that the small input offsets are not magnified by the large OPAMP open-circuit gain.

Comparator:

The comparator again uses an OPAMP in its feedback configuration and a couple of Zener diodes in back-to-back configuration.

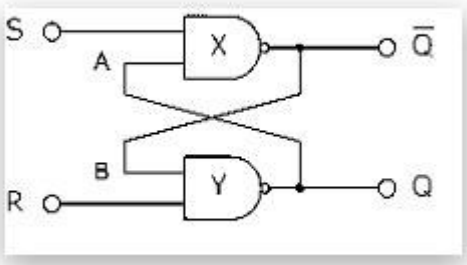
The figure below depicts the implementation of the comparator using back-to-back zener diodes:



Since the amplitude of the detected signal is decoupled from the subsequent outputs at the Ex-OR gate itself, the threshold voltage VREF (or Vth) used in the comparator remains constant for a wide range of values for the incoming optical power.

RS flip-flop:

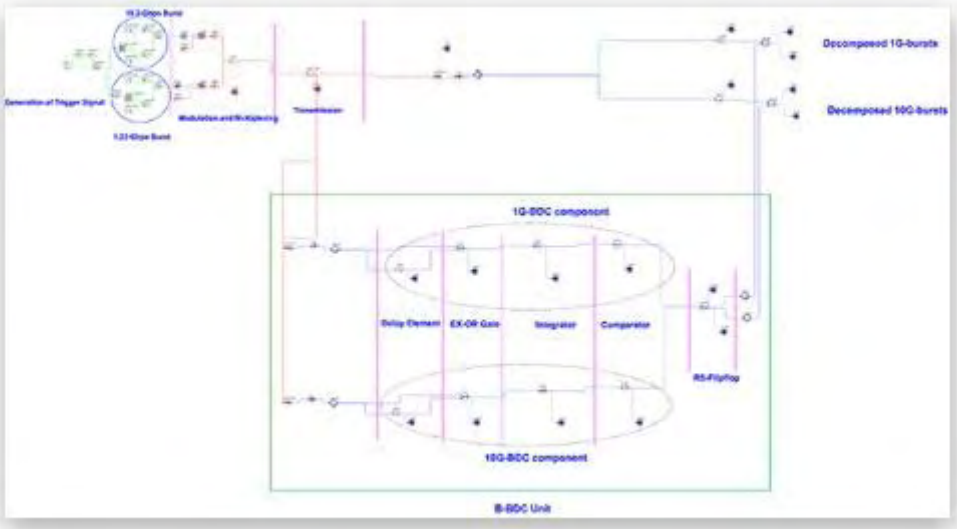
The RS flip-flop implemented here is a basic NAND-latch. The figure below depicts the implementation of RS-flipflop as a basic NAND latch:



There is also a NOT-AND combination gate just before the NAND latch, to make sure the Reset-Set inputs are not active both at the same time.

Figure 1 shows the layout of the project example "Project_BDC_BMRx.moml" implementing the Burst-mode receiver below:

The figure below gives the schematic of the project layout "Project_BDC_BMRx.moml":



On the receiver side, the Burstmode-Bitrate Discrimination Circuit (B-BDC) containing the two arms of 1G and 10G-BDCs is at the bottom of the schematic. The output gate pulses of this B-BDC are used to separate out the data bursts of different bitrates shown at the top-right portion of the layout. Notice

that the received signal is passed through a delay element (whose delay time T_delay is just about the guard time) before combining it with the BDC gate outputs, because the RS flip-flop output switches with some delay (called the response time of the receiver) and thus the gating signal goes well into the start of the next burst if we do not delay the data signal.

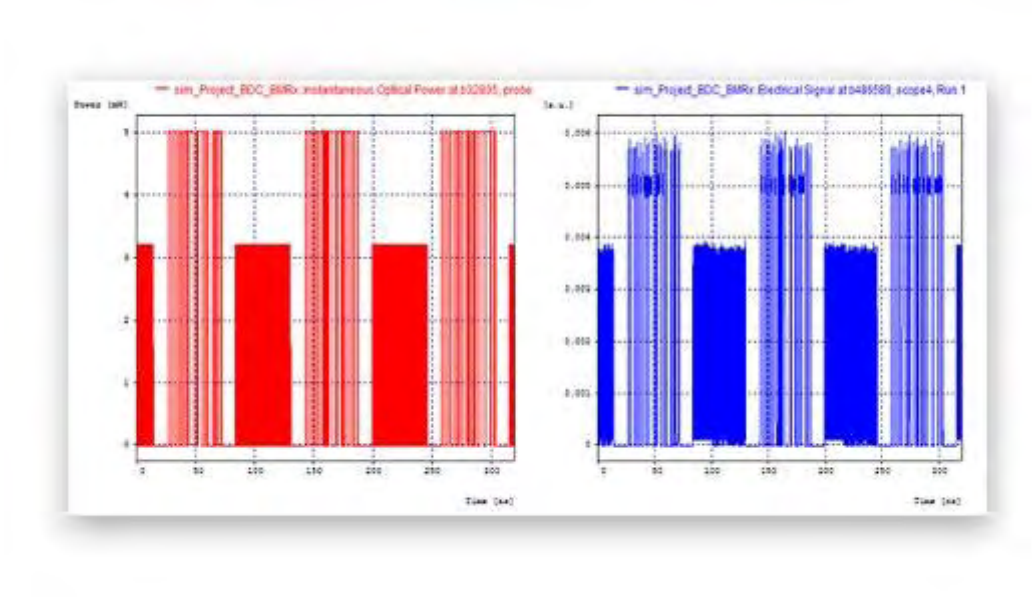
The project simulates dual rate burst packets of 1.25Gbps and 10.3Gbps respectively. The values of the system parameters used here are:

- Length of each burst (burst_len): 58ns
- Preamble length (preamble_len) of 16ns, Payload length (payload_len) of 30ns and a Guard length (guard_len) of 12ns
- Fiber Length (length): 10kms
- Dispersion parameter (disp) at the carrier frequency (1550nm): 16ps/nm//km
- Fiber Loss (loss): 0.1dB/km

The project is simulated for a total simulation time span of about 320ns with a VBS Bandwidth of 0.1236THz.

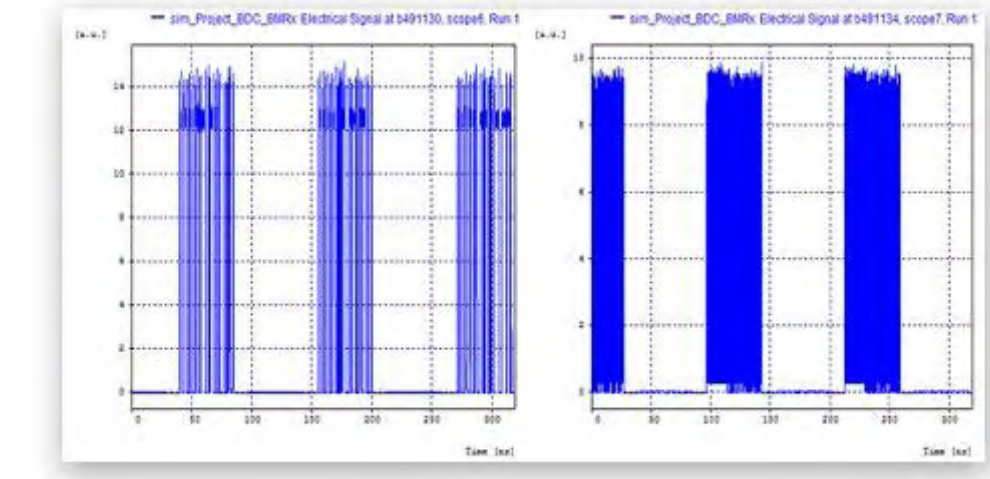
The transmitted composite signal and the received composite signal before the B-BDC component at the receiver are shown below:

The figure below shows the transmitted and the received composite signals



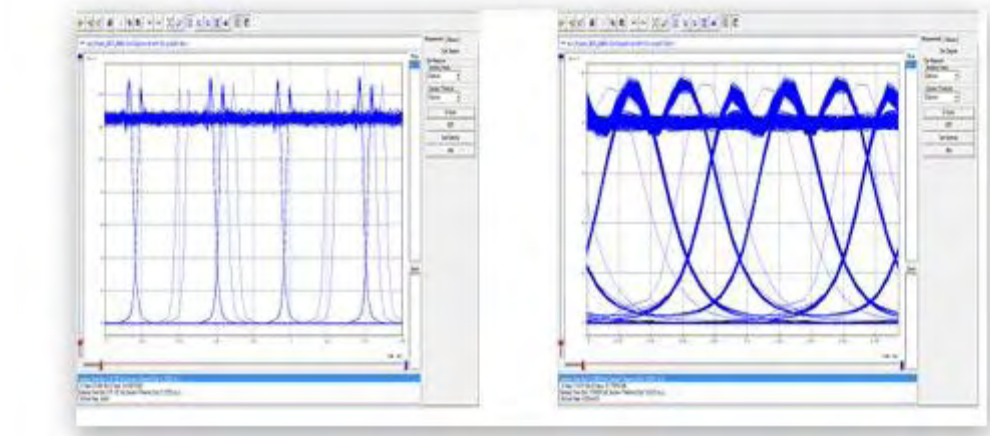
The outputs of the separated 1.25G and 10.3G data burst signals are shown below:

The figure below shows the separated burst signals with 1.25 and 10.3Gbps bitrates respectively



The eye diagrams for the separated out 1.25G and 10.3G data burst signals are shown below:

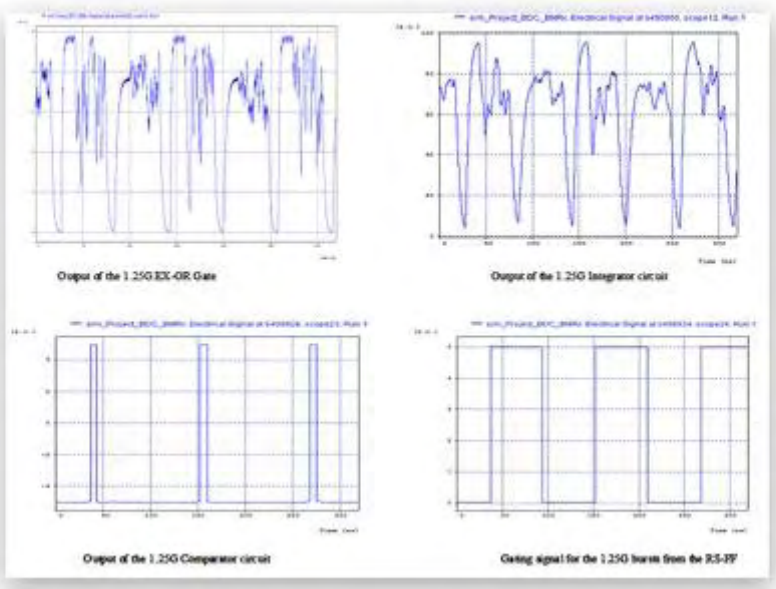
The figure below shows the eye-diagrams of the received 1.25Gbps and 10.3Gbps bitrates respectively



The corresponding BER values shown at the bottom of the figures are about 1E-40 for each bitrate, which is almost 0.

To further illustrate the exact working of this BDC based dual rate burst mode receiver, we show below, the outputs of each of the CCS components implementing the EX-OR gate, Integrator, Comparator and the RS flip-flops respectively for 1G-BDC.

The figure below gives the outputs of the individual CCS components for the 1.25Gbps signal



The results show that the response time for the burst mode receiver (time taken to react and distinguish between the different bitrates) is about 7ns for a burst length of 58ns.

Also, the values of the Resistor (R2) and Capacitor (C1) used in the circuit files of the CCS components simulating the OPAMP based integrator circuits decide the value of the time constant of the integrator output, and hence might sometimes require fine-tuning if the burst length specifications are considerably changed.

The BM receiver components can easily be customized for use in any dual-rate burst-mode project with different bitrate values, by changing the delay time values for the delay elements used just before the first CCS components of both arms implementing the EX-OR gates. The values for the delay time T_delay must be 1/bitrate for the alternating preamble sequence ("01010...") and 2/bitrate for the cyclic preamble sequence ("01100110...").

In case the preamble sequence is changed, an appropriate logical circuit must be designed for it and implemented using the first CCS component that implements the EXOR gate currently.

References

[1] Kazutaka Hara, Shunji Kimura, Hirotaka Nakamura, Naoto Yoshimoto, and Kiyomi Kumozaki, "Burst-mode Bit-rate Discrimination Circuit for 1.25/10.3-Gbit/s Dual-rate PON Systems", OFC 2009, Optical Society of America conference (2008).