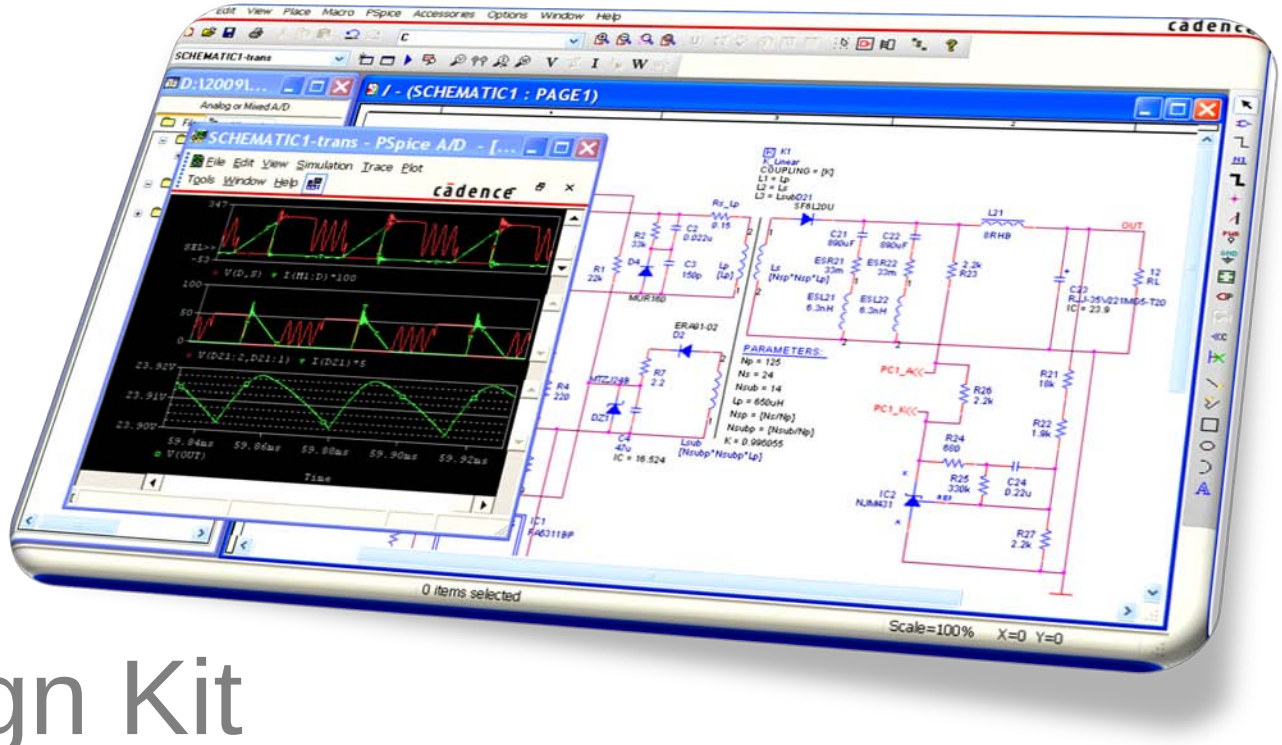


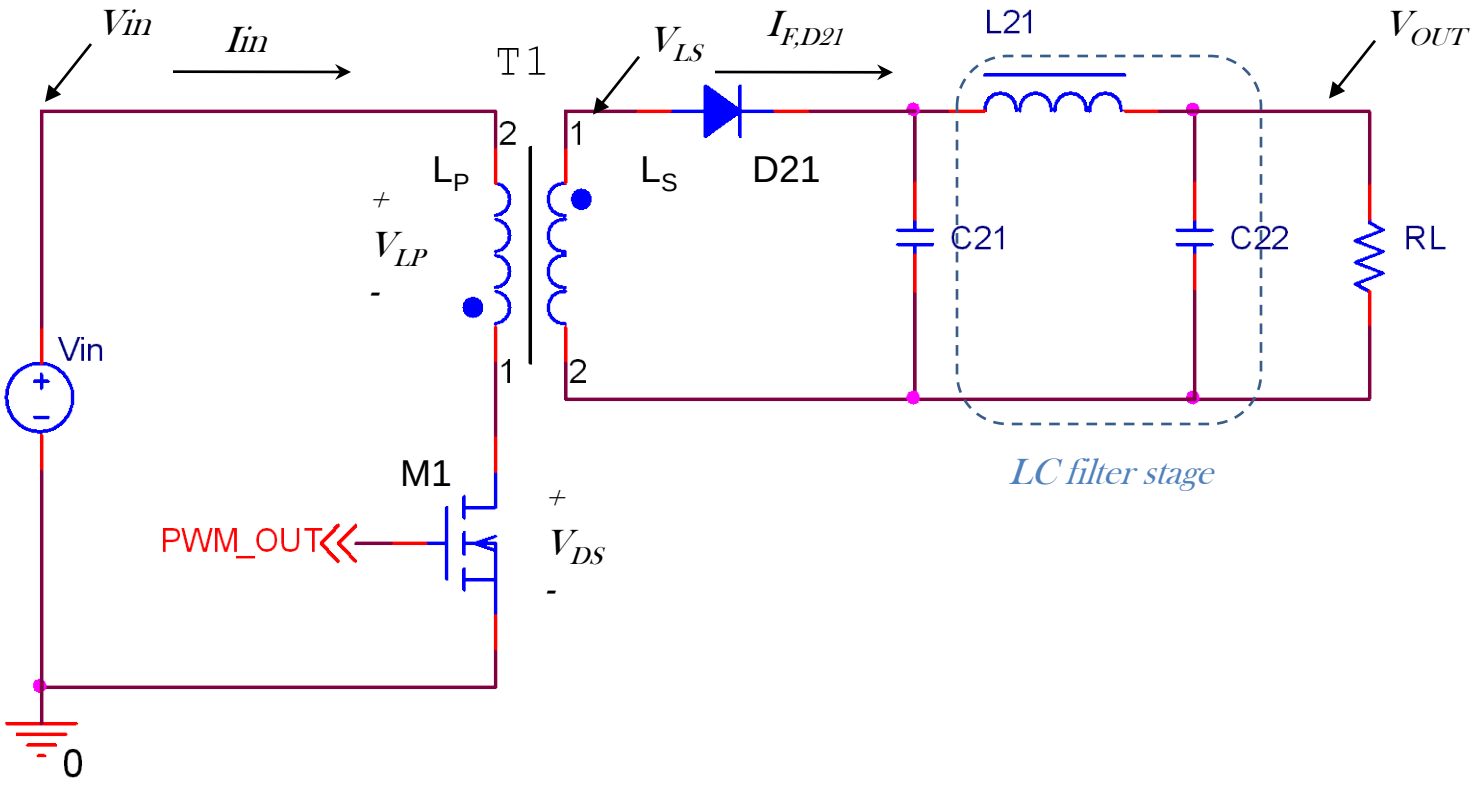
Design Kit

Fixed Frequency Switch Mode Power Supply Using FA5311BP

Contents (1/2)

Contents (2/2)

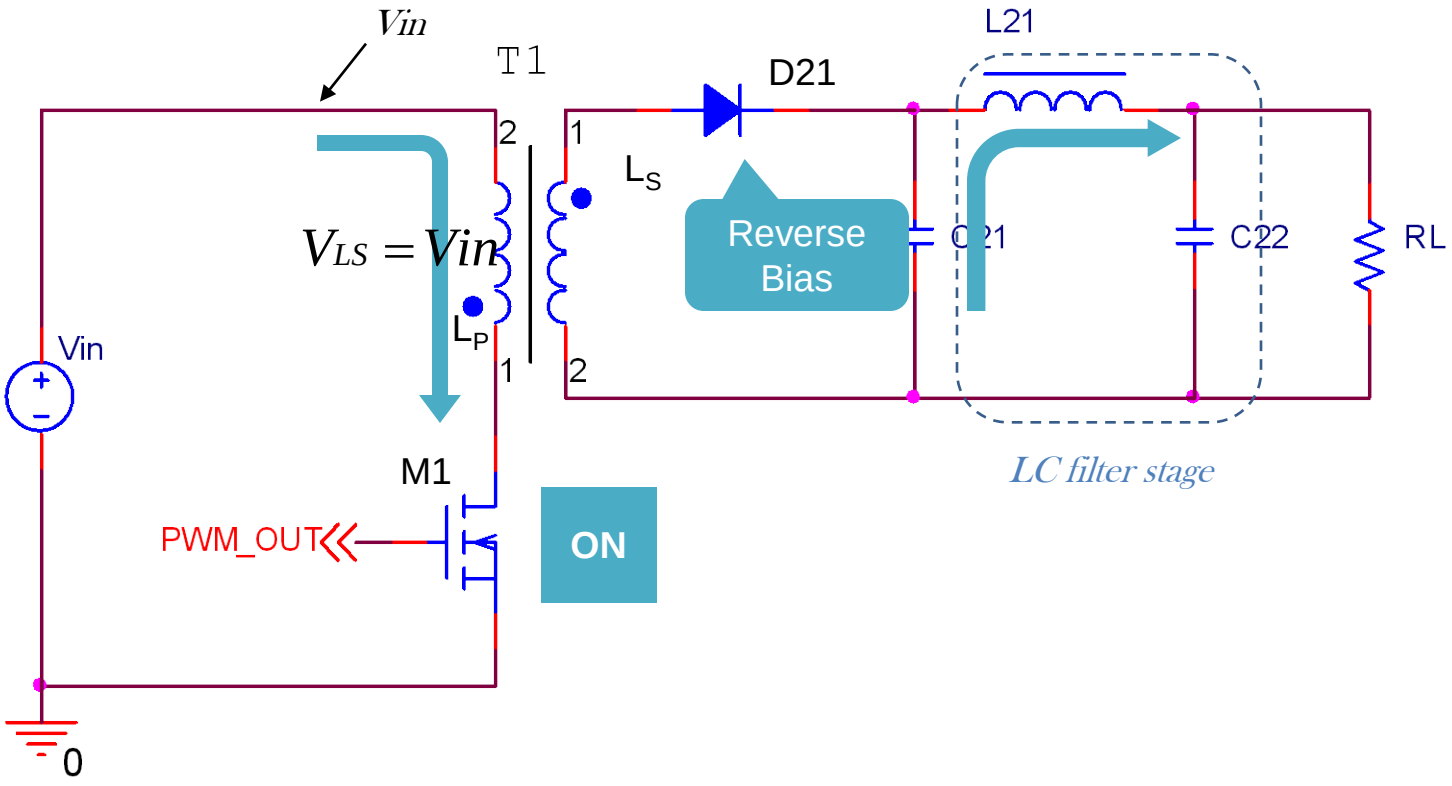
1.1 Flyback Converter



- This figure shows the basic configuration of the converter (Flyback + LCR load).
- The switch M1 ON and OFF events are separated to see how the devices work.

1.1 Flyback Converter

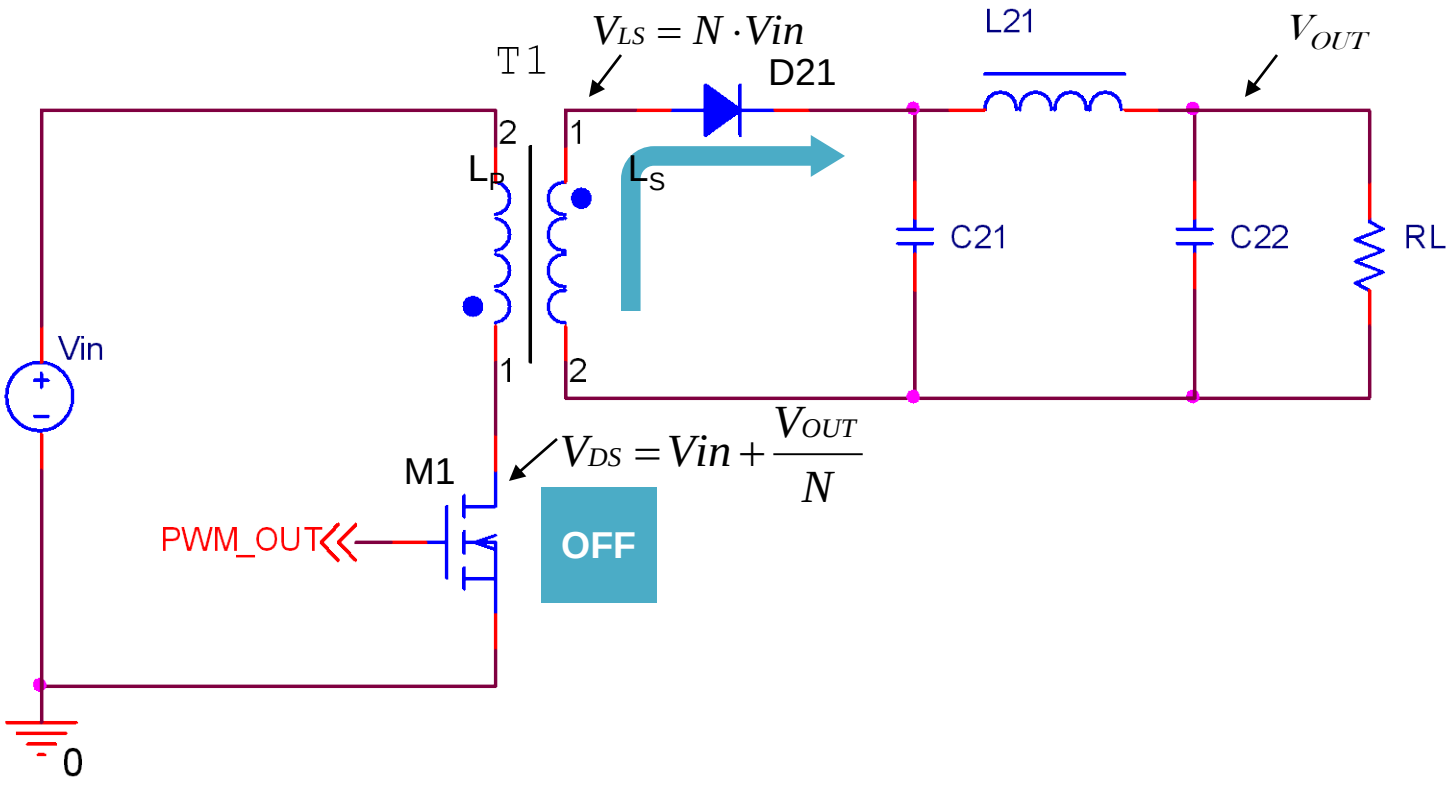
During the M1 ON time



- This figure shows the current path during the ON time, D21 is reverse biased, and the output capacitor (C21) supplies the LC filter stage on its own.

1.1 Flyback Converter

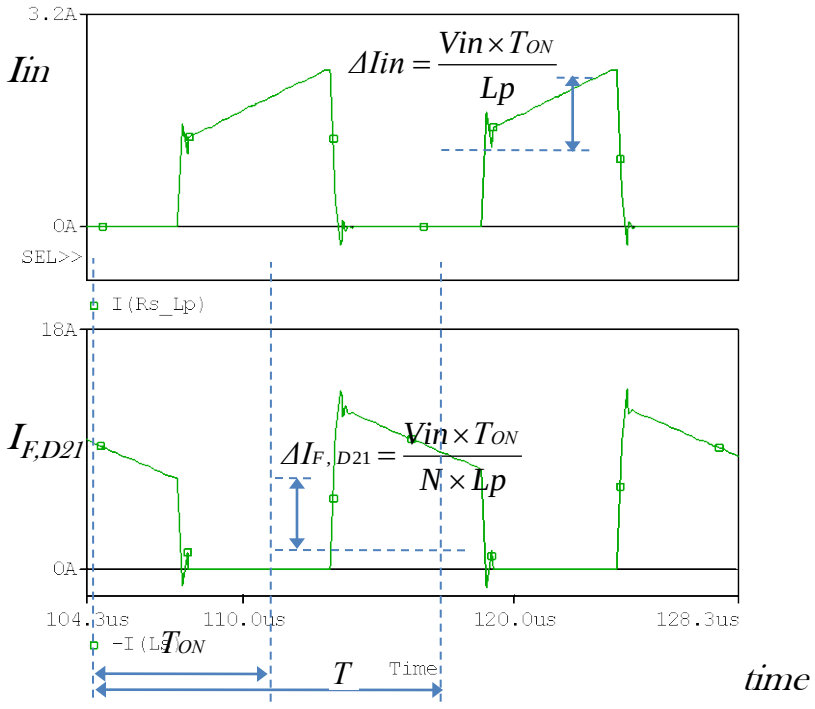
During the M1 OFF time



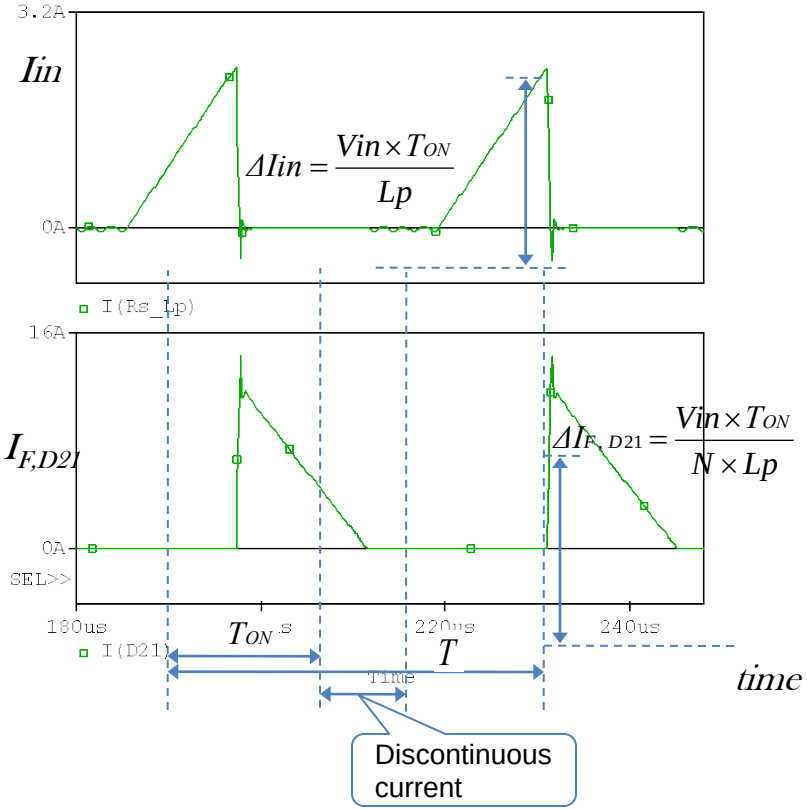
- During the OFF time, D21 is forward biased , L_S starts conducting and charges C21 ,the secondary winding of the flyback transformer starts transferring energy to the power supply output.

1.2 Current Waveforms

CCM



DCM



- The current waveforms of Iin and $I_{F,D21}$ in CCM and DCM mode.

1.3 Equations

- The relationship between the V_{OUT} and V_{in} for the CCM and DCM mode are defined as equations below.

$$V_{OUT,CCM} = \frac{N_S}{N_P} \cdot \left(\frac{D}{1-D} \right) \cdot Vin \qquad (1)$$

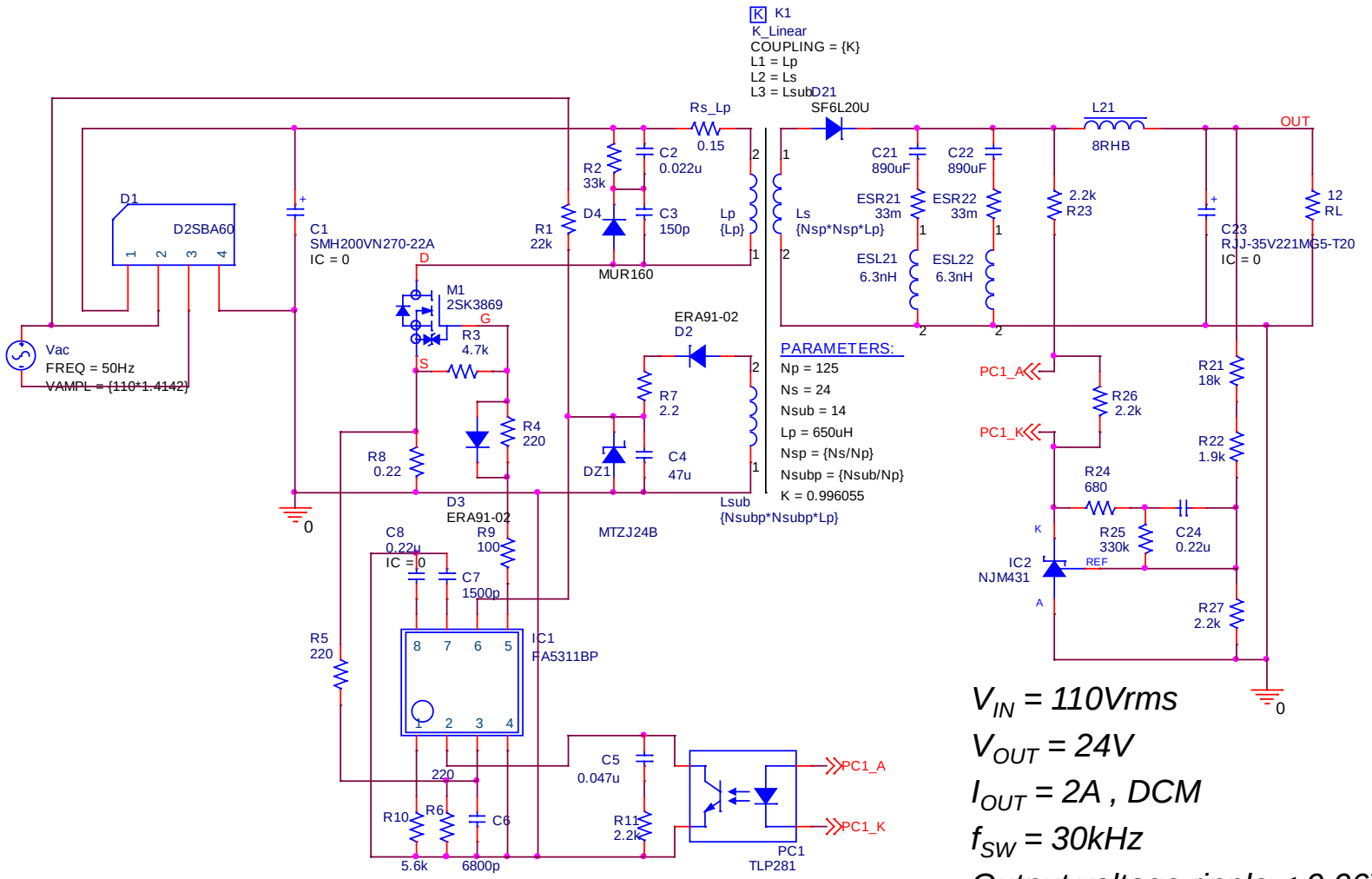
$$V_{OUT,DCM} = D \times Vin \times \sqrt{\frac{R_L}{2 \times L_P \times f_{sw}}} \qquad (2)$$

- The primary side inductance value L_P for the DCM mode is calculated as equation below.

$$L_{P,DCM} < \frac{(1-D)^2 R}{2 f_S} \cdot \left(\frac{N_P}{N_S} \right)^2 \qquad (3)$$

  - L_P is the inductance of primary winding.
  - $D = T_{ON} / T$
  - N_P is the turns number of primary winding.
  - N_S is the turns number of secondary winding.

2. Specifications



V_{IN} = 110Vrms

V_{OUT} = 24V

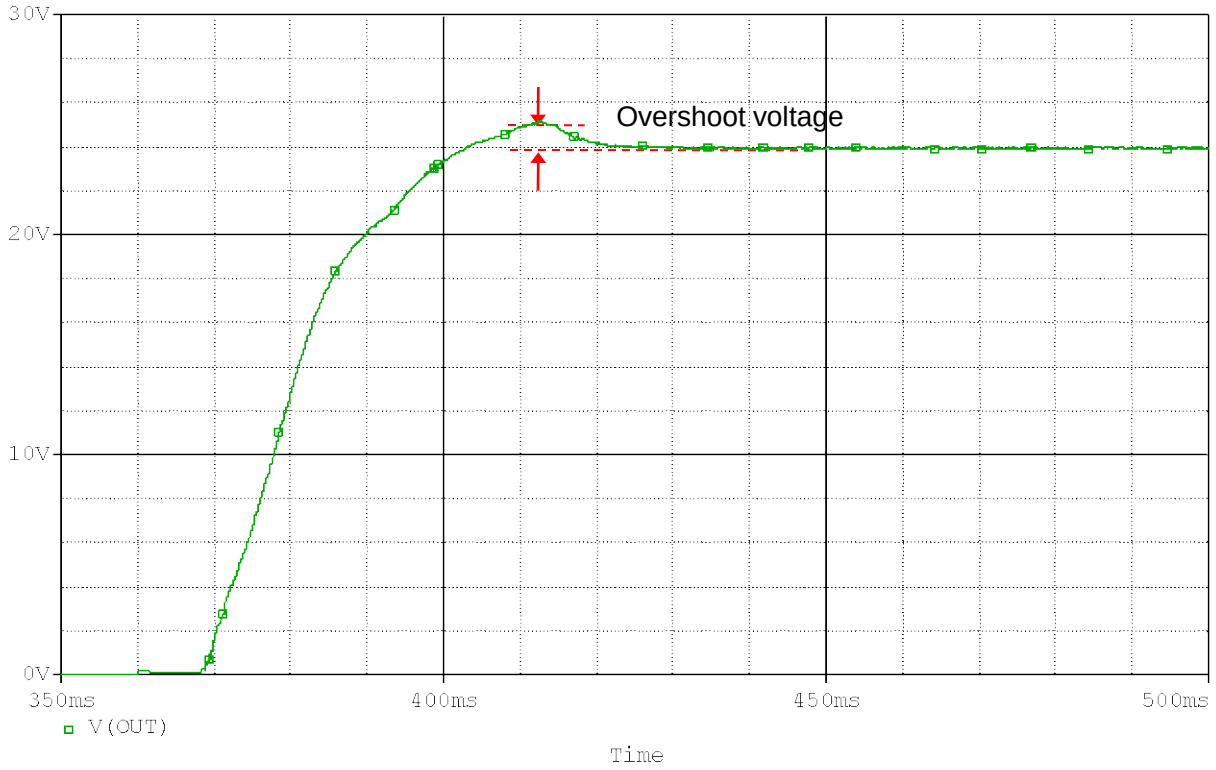
I_{OUT} = 2A , DCM

f_{SW} = 30kHz

Output voltage ripple < $0.06V_{P-P}$

%Efficiency = 85.6

2.1 Output Voltage



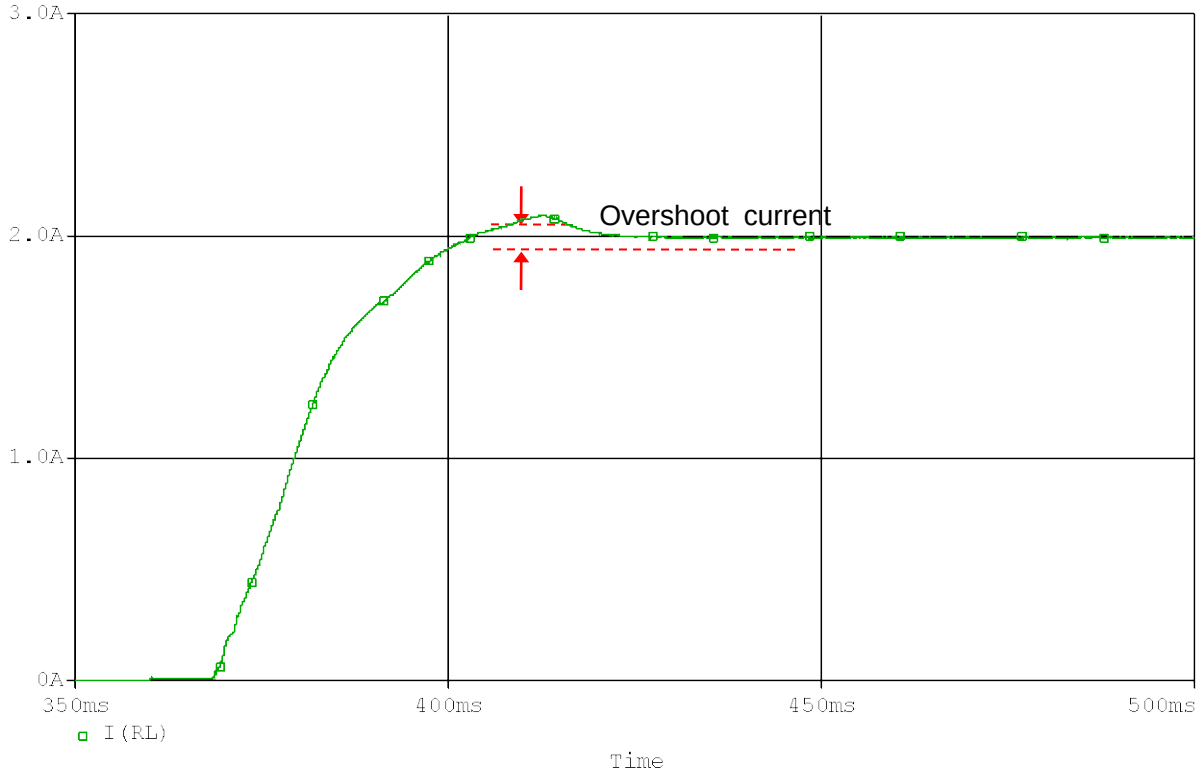
Analysis
Time Domain (Transient)
Run to time: 500ms
Start saving data after: 0
Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- The output voltage is regulated at 24V(RL=12Ω) ,voltage overshoot at startup is less than 1.2V.

2.2 Output Current



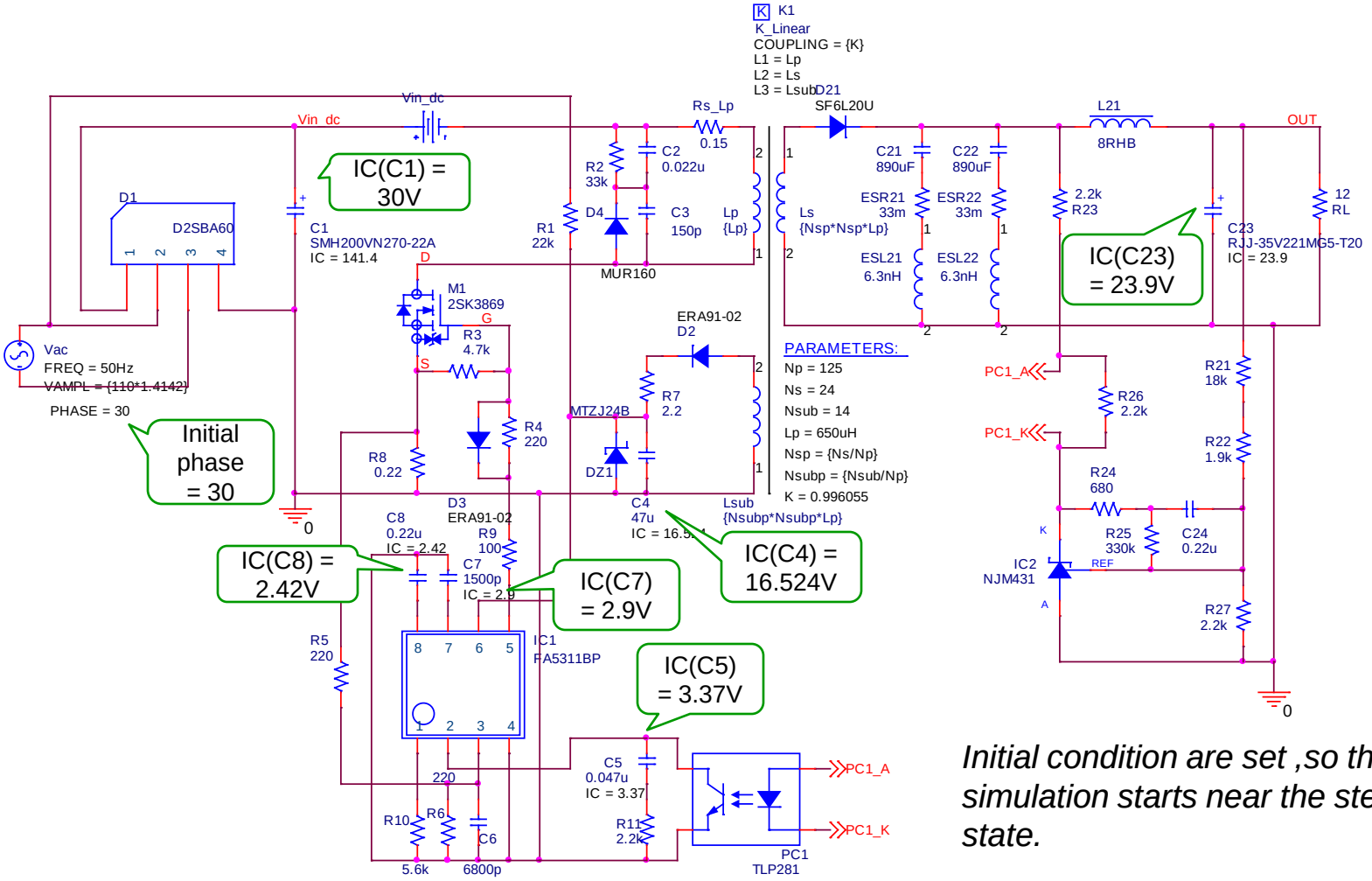
Analysis
Time Domain (Transient)
Run to time: 500ms
Start saving data after: 0
Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

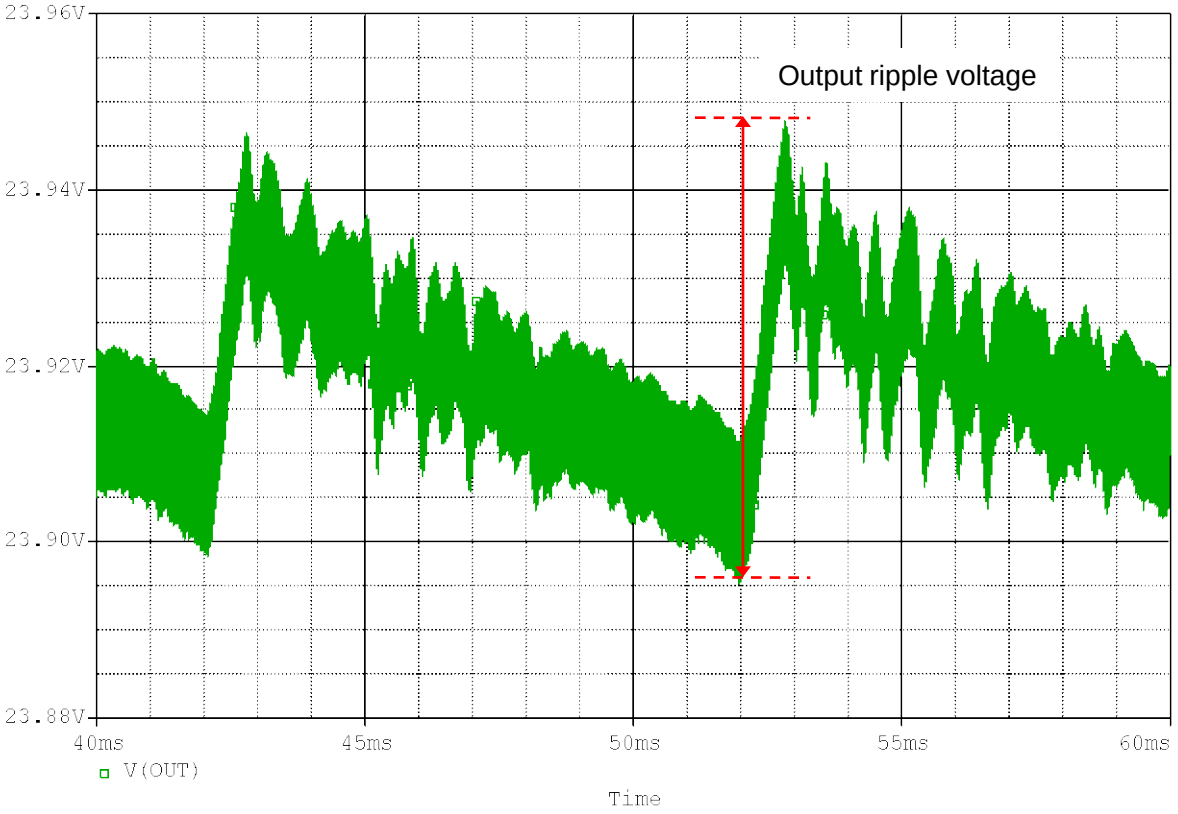
- The output current is 2A (RL=12Ω) ,current overshoot at startup is less than 100mA.

2.3 Steady State Initial Conditions



Initial condition are set ,so the simulation starts near the steady state.

2.4 Output Ripple Voltage



Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

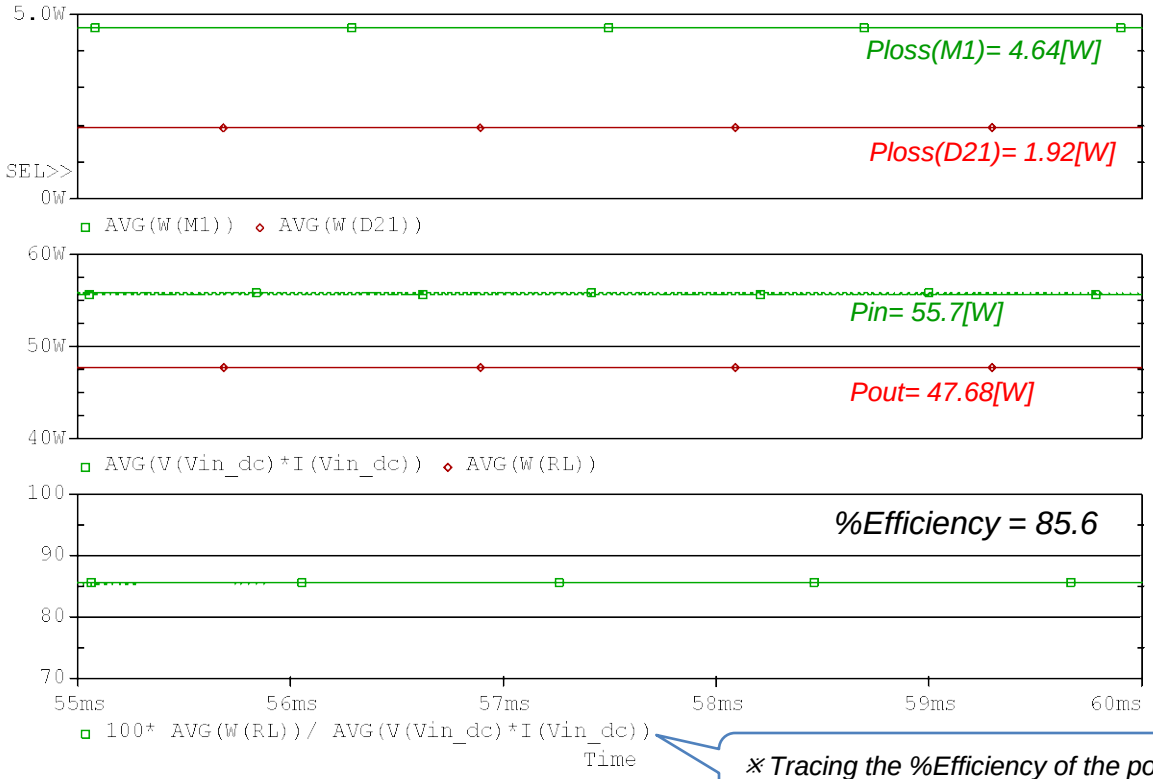
.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- The output ripple voltage is less than 60 mV_{P-P}.

2.5 Efficiency

※ *Tracing the %Efficiency of the power supply ,add trace: 100* AVG(W(RL))/ AVG(V(Vin_dc)*I(Vin_dc))*



Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

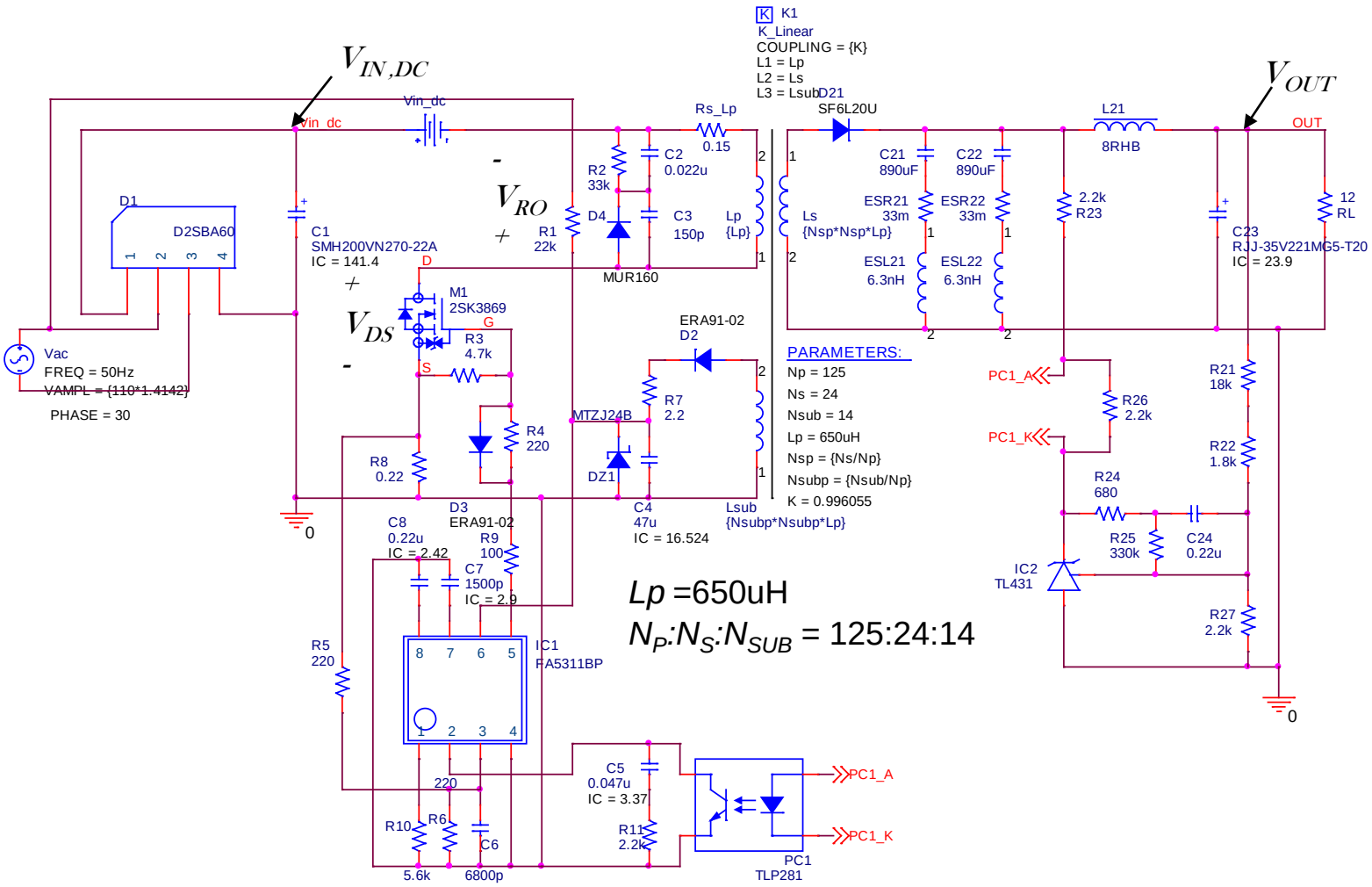
.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

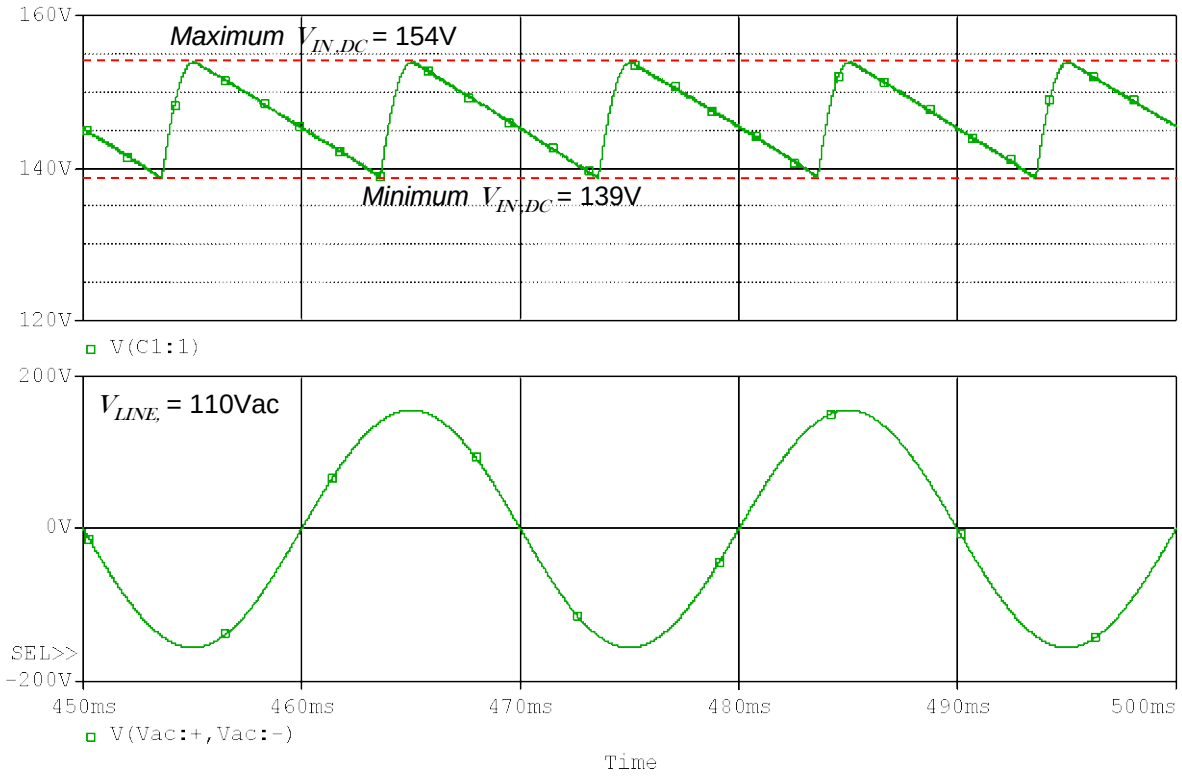
※ *Tracing the %Efficiency of the power supply ,add trace: 100* AVG(W(RL))/ AVG(V(Vin_dc)*I(Vin_dc))*

- The simulation result shows that the efficiency of the power supply is 85.6%.

3. Design Considerations



3.1 DC Link Voltage $V_{IN,DC}$



Analysis

Time Domain (Transient)

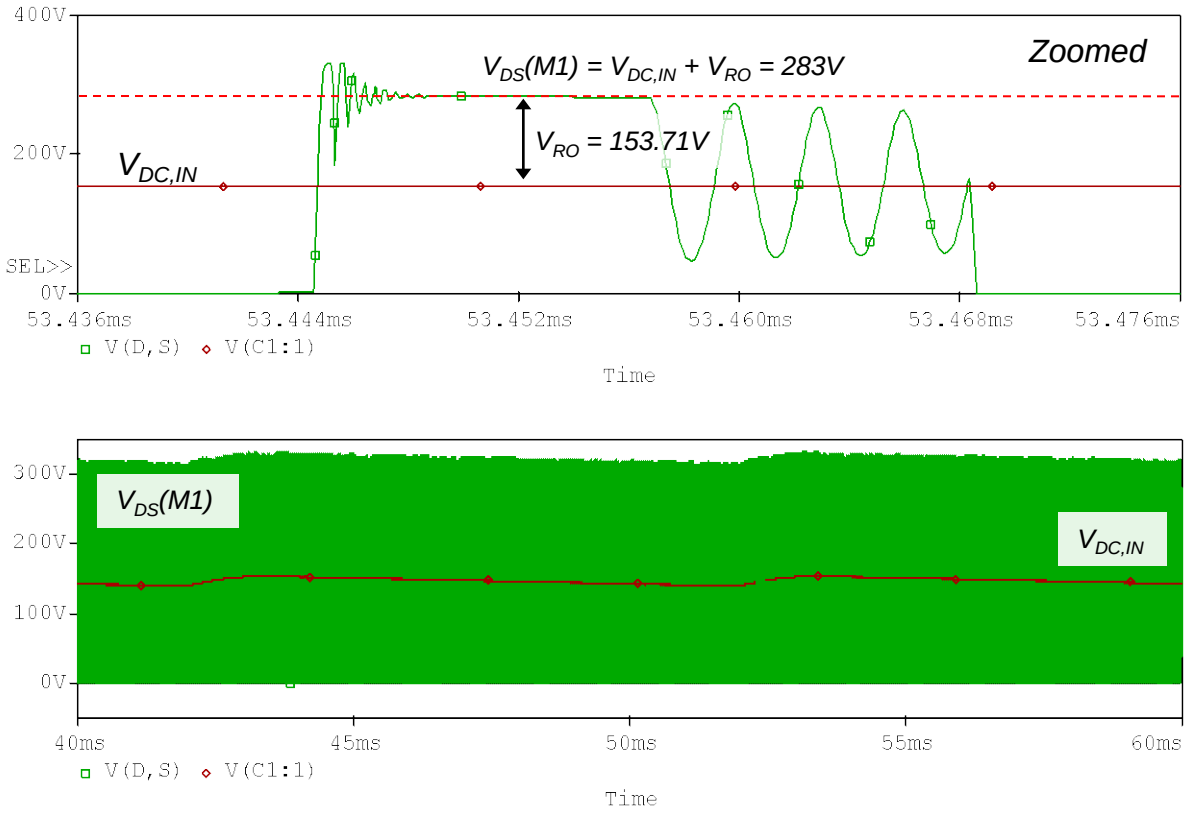
- Run to time: 500ms
- Start saving data after: 0
- Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- The simulation result shows the peak values of the ripple of DC link voltage $V_{IN,DC}$.

3.2 Reflected Voltage V_{RO}



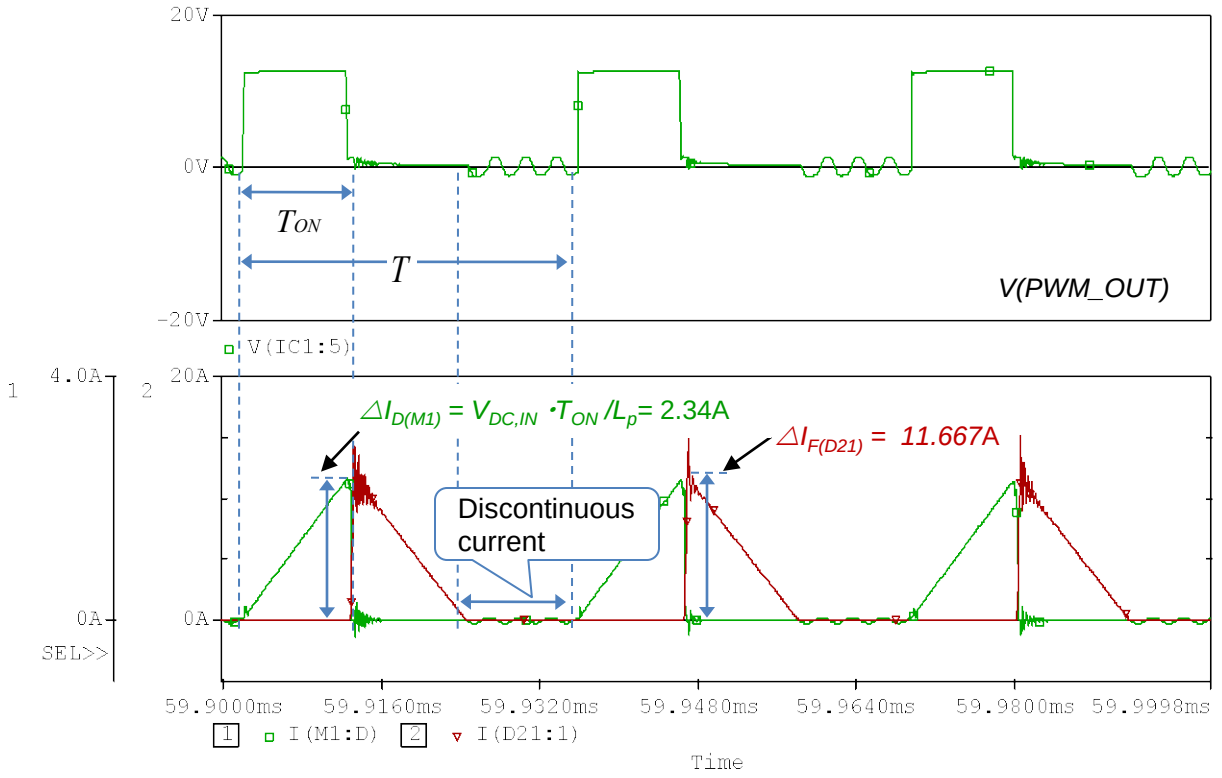
Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- This figure shows the waveform of the drain voltage of flyback converter compared to the $V_{DC,IN}$.
- When M1 is turned off ,$V_{DS} = V_{DC,IN} + V_{RO}$
- V_{RO} is the voltage reflected to the primary, the value is approximately V_{OUT} / N ,*which* $N=N_S/N_P$

3.3 Transformer Primary Side Inductance L_P



Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- This figure shows the waveforms of $I_{D(M1)}$ and $I_{F(D21)}$ in the DCM mode. The peak currents are obtained.
- The primary-side inductance (L_P) of the transformer determines the converter operation mode.
- Once the duty ratio is determined by the equation (1), L_P is obtained as the equation (3)
- Which the maximum load is 2A (V_O=24V, R_L=12Ω). At $V_{IN,dc}$=141V and f_s=30kHz ,this equation calls for $L_{p,DCM}$ < 1.52mH.

3.4 Transformer Turn Ratio

The turn ratio between the primary side and the secondary side is obtained as:

$$\frac{N_S}{N_P} = \frac{V_{OUT} + V_{F(D21)}}{V_{RO}} \qquad (4)$$

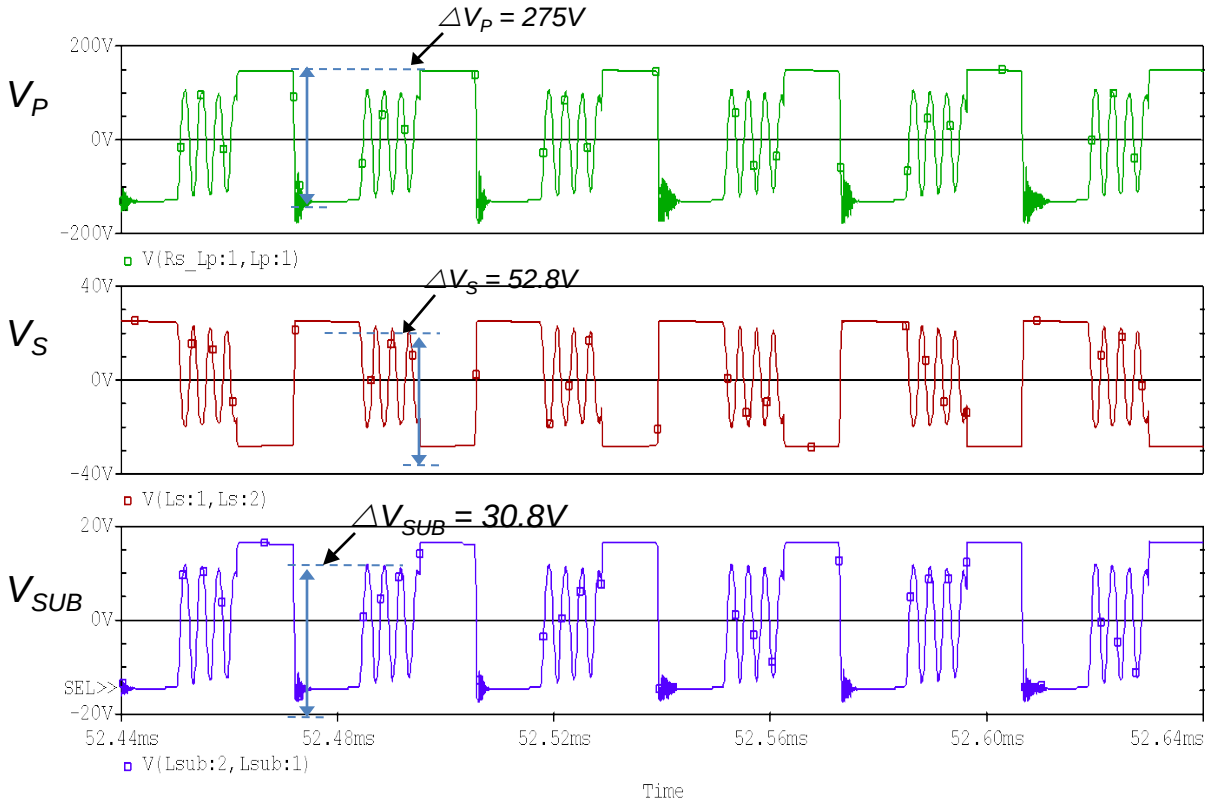
The turn ratio between the primary side and the auxiliary side is obtained as:

$$\frac{N_{SUB}}{N_S} = \frac{V_{CC} + V_{F(Dsub)}}{V_{OUT} + V_{F(D21)}} \qquad (5)$$

Which the maximum load current is 2A (V_O=24V, R_L=12Ω).

- At $V_{F(D21)}$≅0.6V and V_{RO}=129V ,this equation calls for N_P:N_S = *125:24.*
- At $V_{F(Dsub)}$≅0.6V and V_{CC}=14V (more than $V_{CC,OFF}$ of FA5311BP) ,this equation calls for N_S:N_{SUB} = *24:14.*

3.4 Transformer Turn Ratio



Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- This figure shows the waveforms of the voltages at each side of the transformer.

3.5 Transformer leakage inductance

- To model the transformer (or coupled inductors), we can use the SPICE primitive k ,which describes the coupling ratio between a primary and a secondary.
- The k value is obtained as:

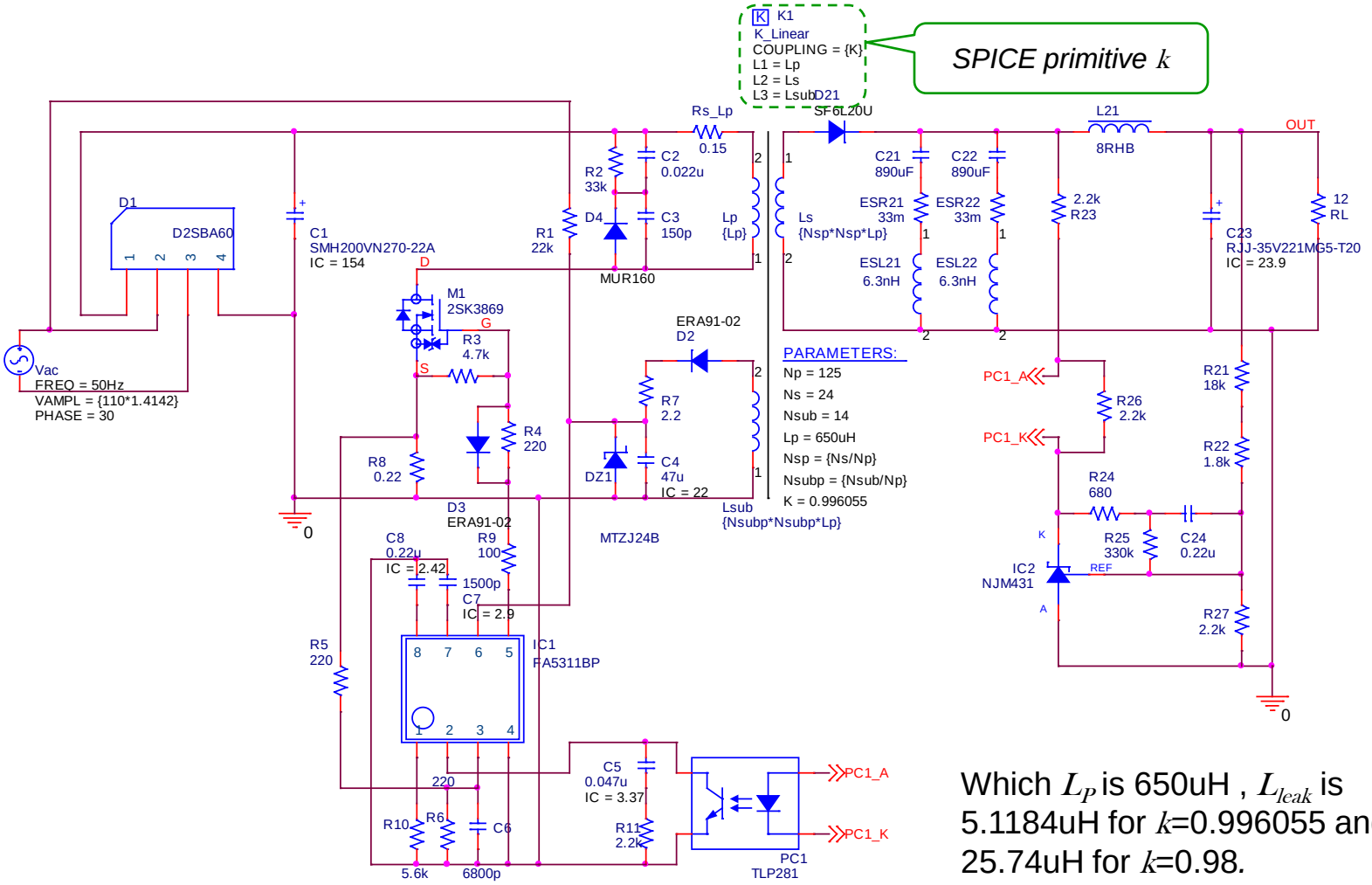
$$k = \sqrt{1 - \frac{L_{P,\,LSS}}{L_{P,\,LSO}}} \qquad (6)$$

  - k is the SPICE primitive which describes the coupling ratio between a primary and a secondary.
  - $L_{P,LSS}$ is the Inductance value of primary winding when the secondary winding is shorted.
  - $L_{P,LSS}$ is the Inductance value of primary winding when the secondary winding is opened.

- The leakage inductance of the transformer L_{leak} is describe as equation:

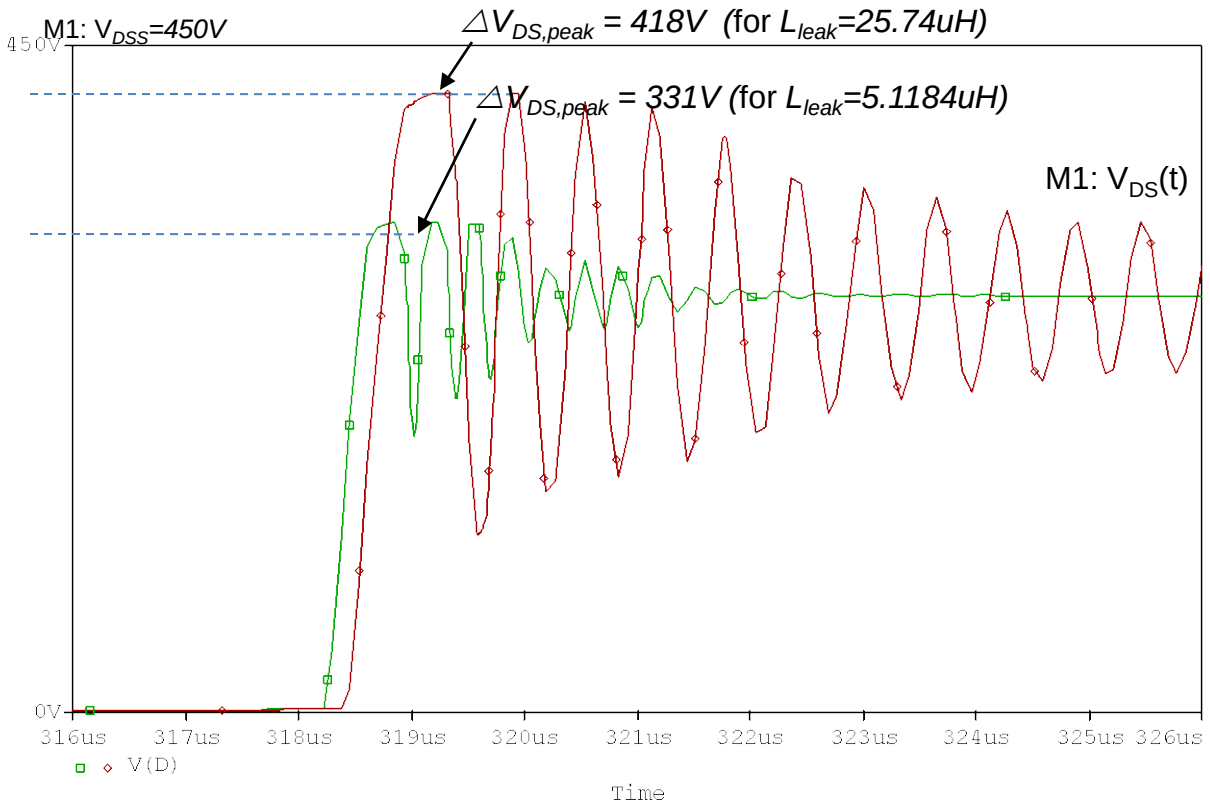
$$L_{leak} = L_P \cdot (1 - k^2) \qquad (7)$$

3.5 Transformer leakage inductance



Which L_P is 650uH , L_{leak} is 5.1184uH for k=0.996055 and 25.74uH for k=0.98.

3.5 Transformer leakage inductance



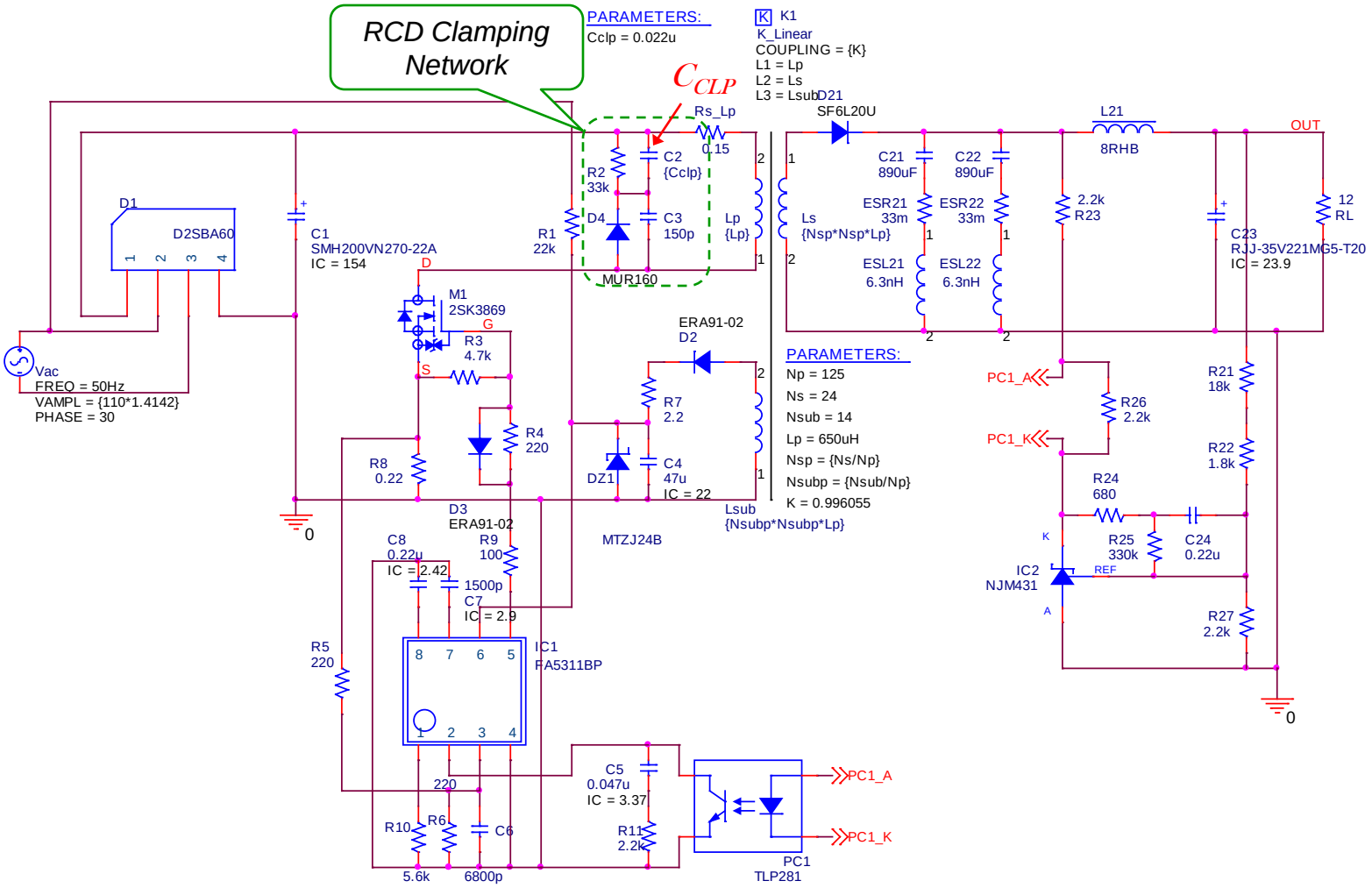
Analysis
Time Domain (Transient)
Run to time: 1000us
Start saving data after: 0
Maximum step size: 80ns
Sweep variable
◉ Global parameter: k
◉ Value list: 0.996055, 0.98

.Options

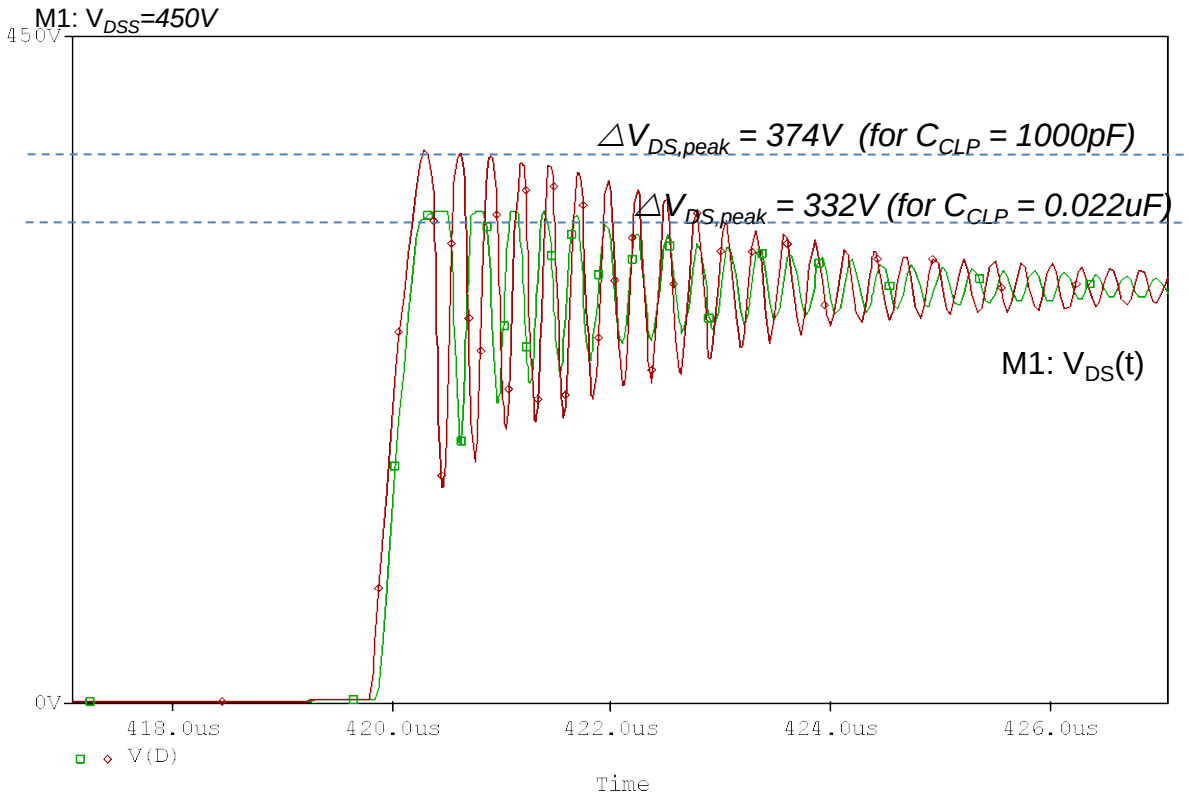
RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation result shows that the smaller L_{leak} gets lower V_{DS} peak voltage ,that means better design margin from the MOSFET V_{DSS}

3.6 RCD Clamping network



3.6 RCD Clamping network



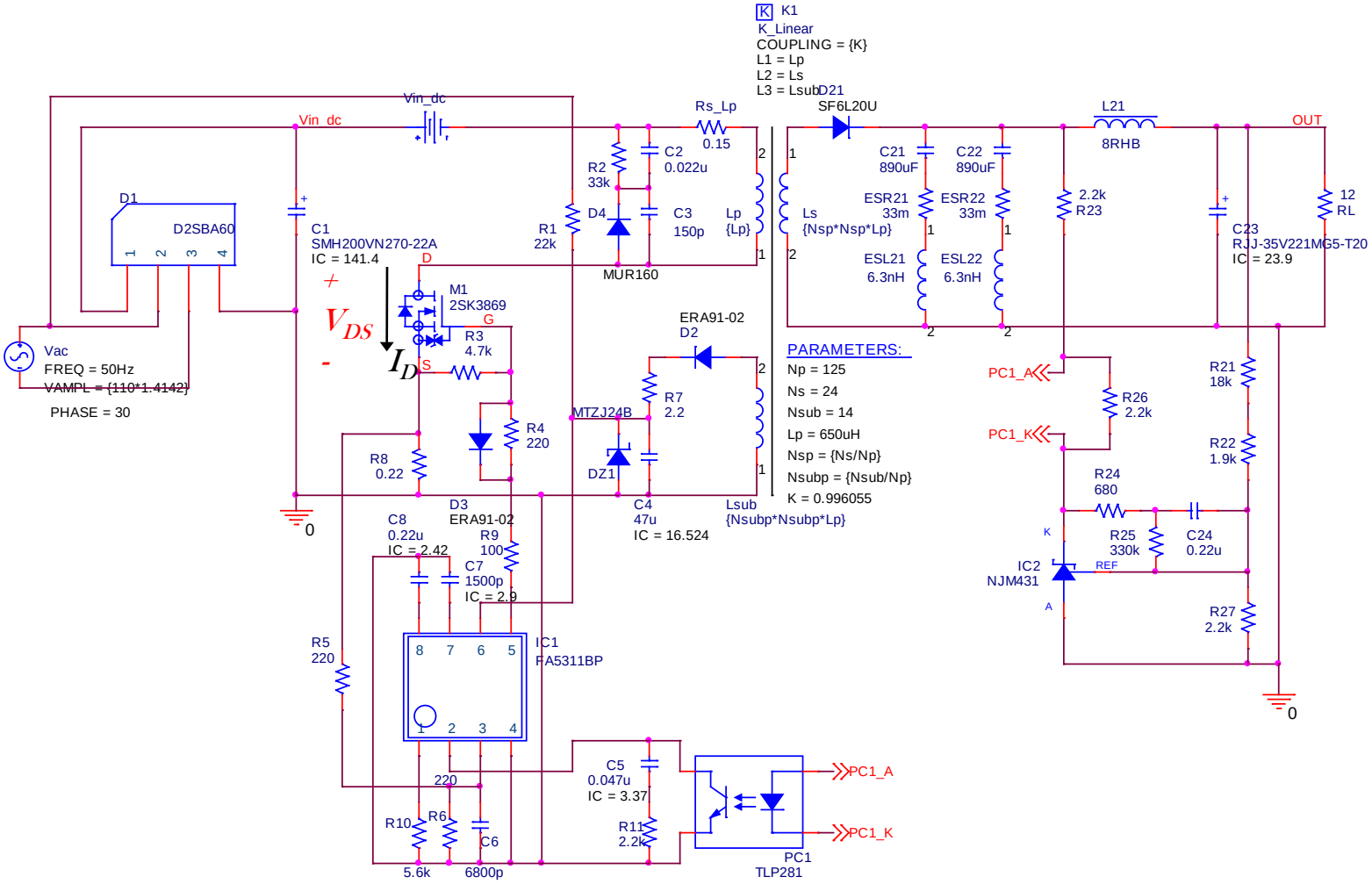
Analysis
Time Domain (Transient)
Run to time: 500us
Start saving data after: 0
Maximum step size: 40ns
Sweep variable
◉ Global parameter: Cclp
◉ Value list: 0.022u, 1000p

.Options

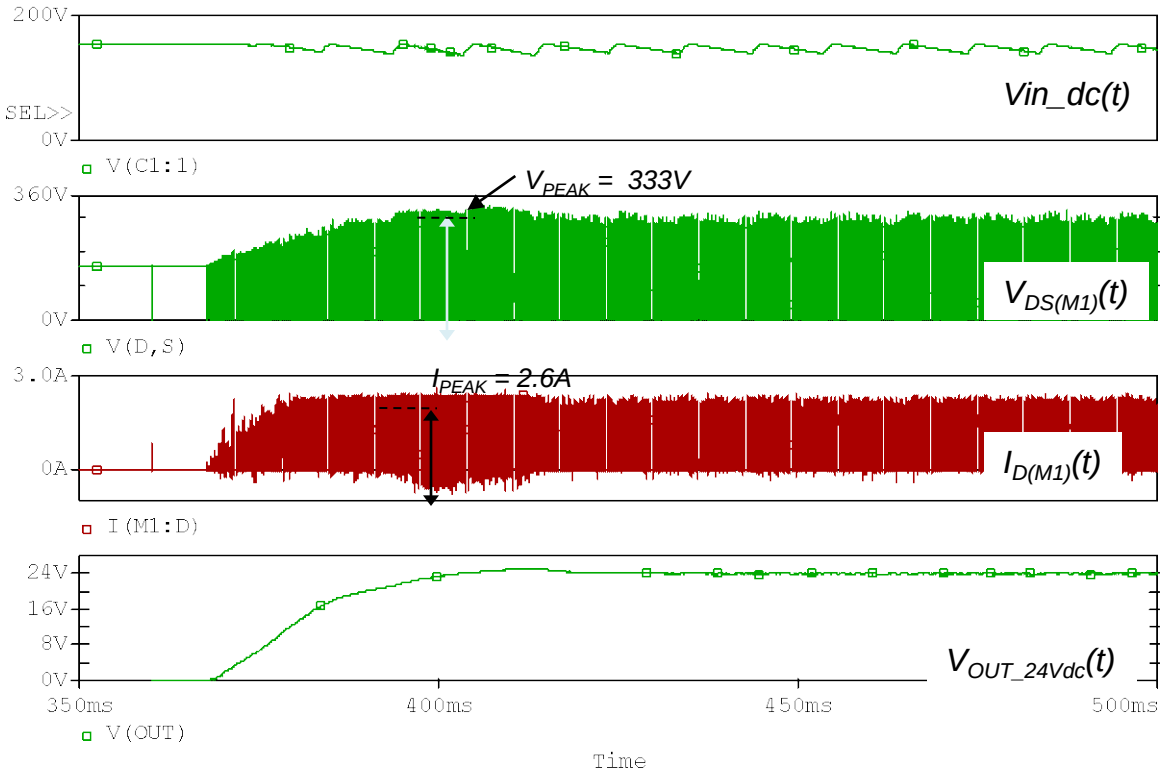
RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation result shows V_{DS} peak voltages for the C_{CLP}(C2) = 0.022uF and 1000pF.
- A larger C_{CLP} value gets lower V_{DS} peak voltage ,that means better design margin from the MOSFET V_{DSS}

4. MOSFET Switching Device M_1



4.1 M_1 Voltage and Current Stresses



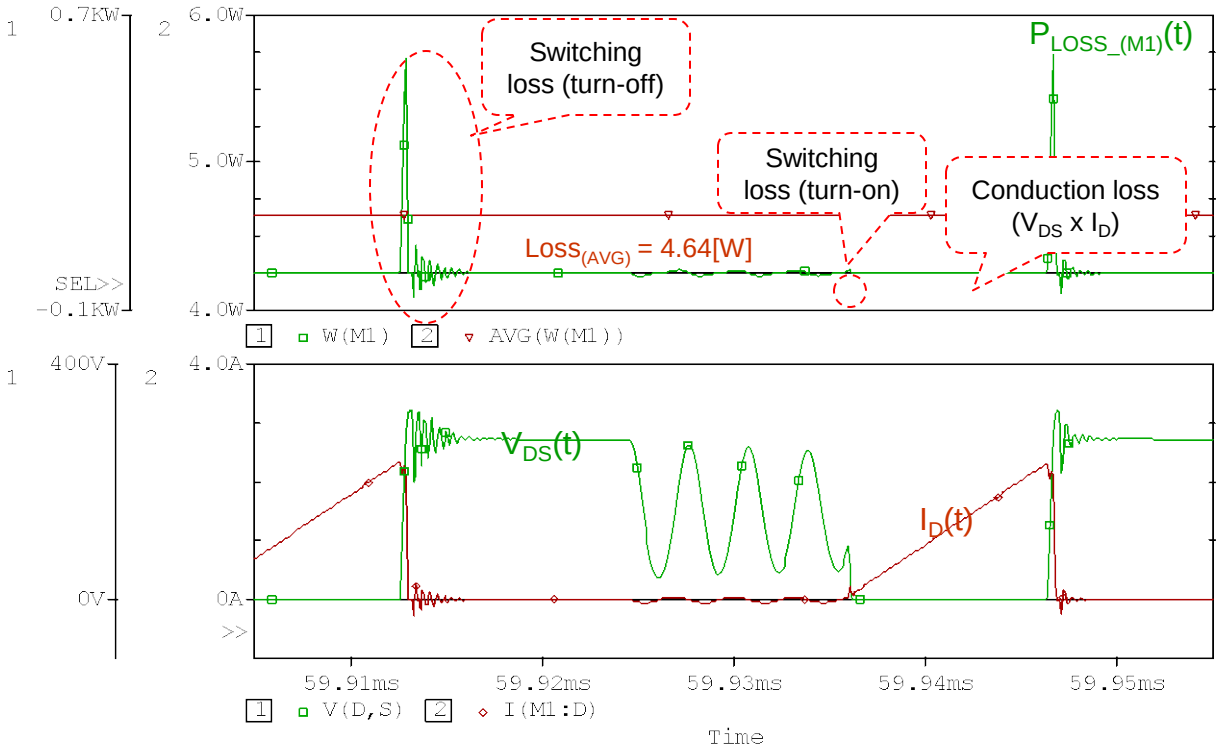
Analysis
Time Domain (Transient)
Run to time: 500ms
Start saving data after: 0
Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation result shows the $V_{DS(M1)}$ peak voltage and the $I_{D(M1)}$ peak current.
- The voltage and current should not exceed the maximum rating of the device M_1 (2SK3869: V_{DSS}=450V , $I_{D,max}$=10A).

4.2 Losses in M_1



Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

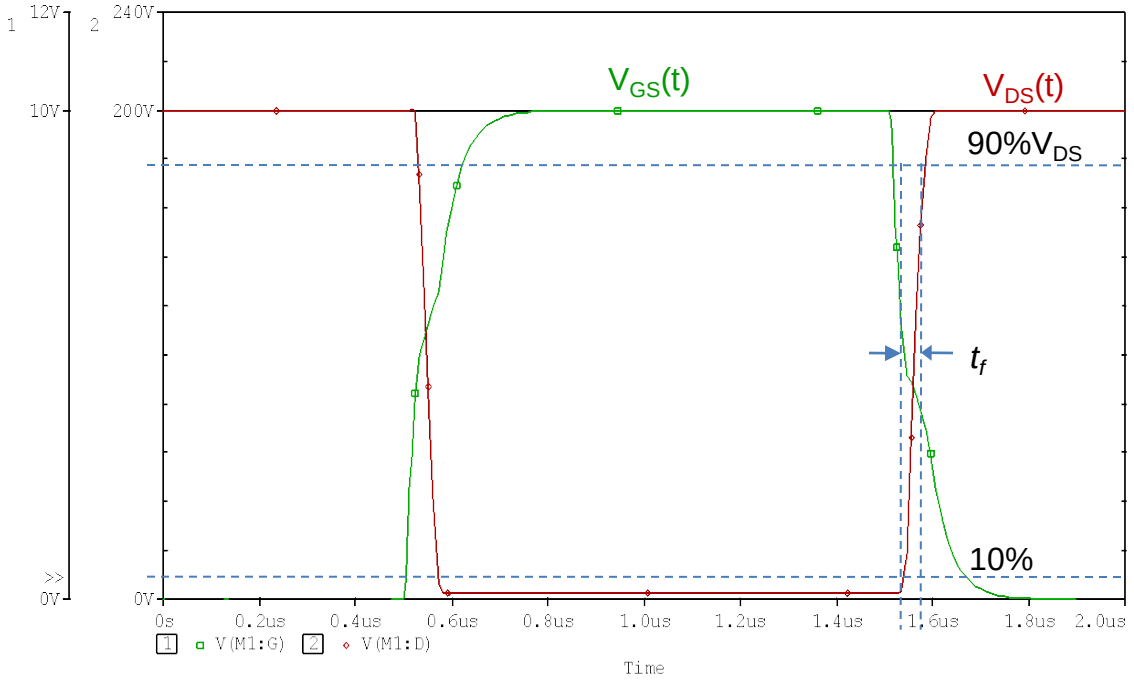
.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation results shows waveforms of I_D and V_{DS} of MOSFET M_1. Switching power loss and average power loss are also shown.

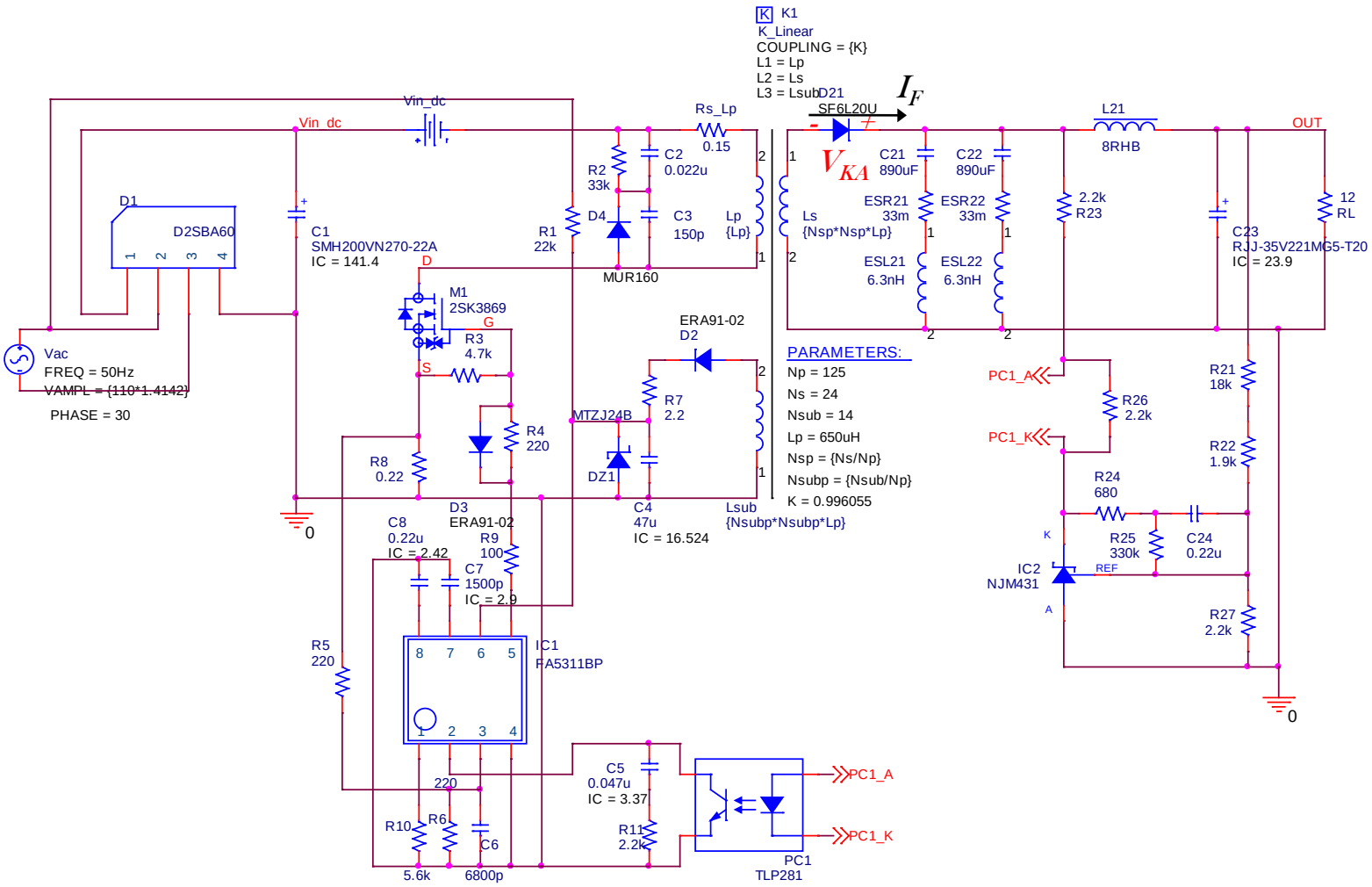
4.3 MOSFET Model

- This figure shows the verification of the MOSFET model with measured fall time characteristics ,that is the key to accurate $P_{LOSS\_(M1)}$ simulation.

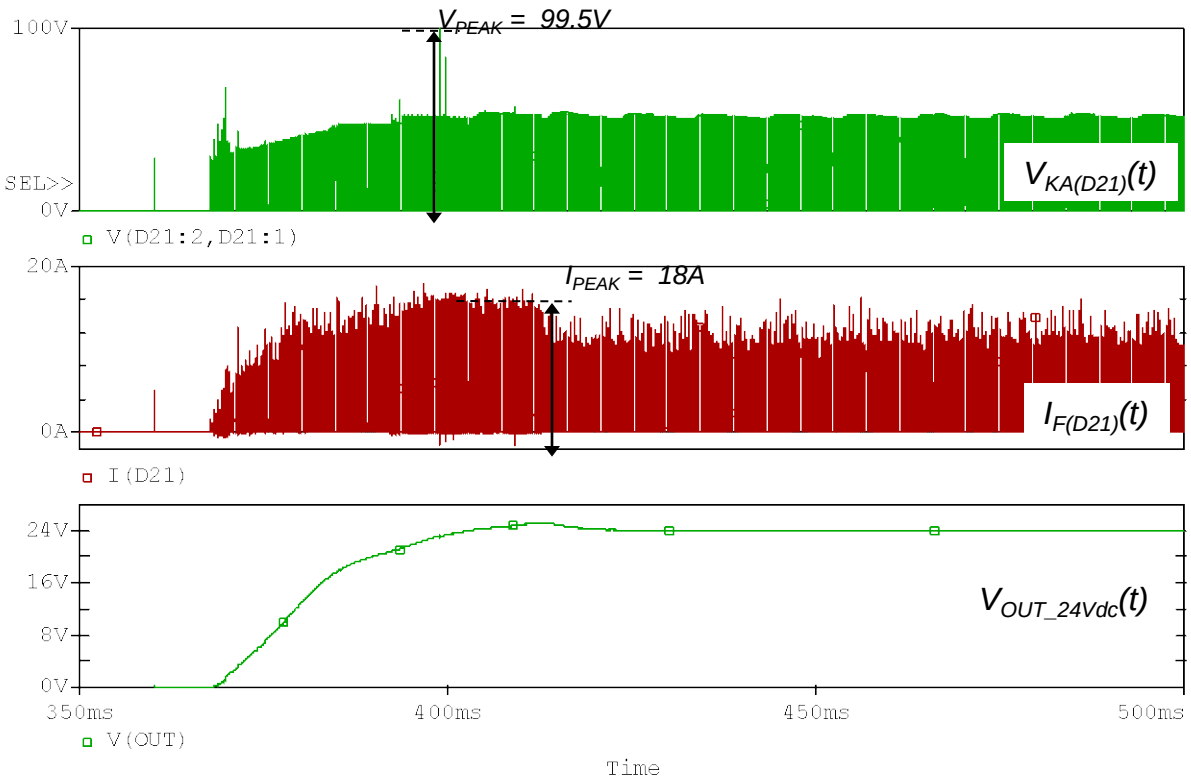


	Measured	Simulated	%Error
Fall time (tf)	40(ns)	38.976(ns)	-2.56

5. Output Rectifier Diode D_{21}



5.1 D_{21} Voltage and Current Stresses



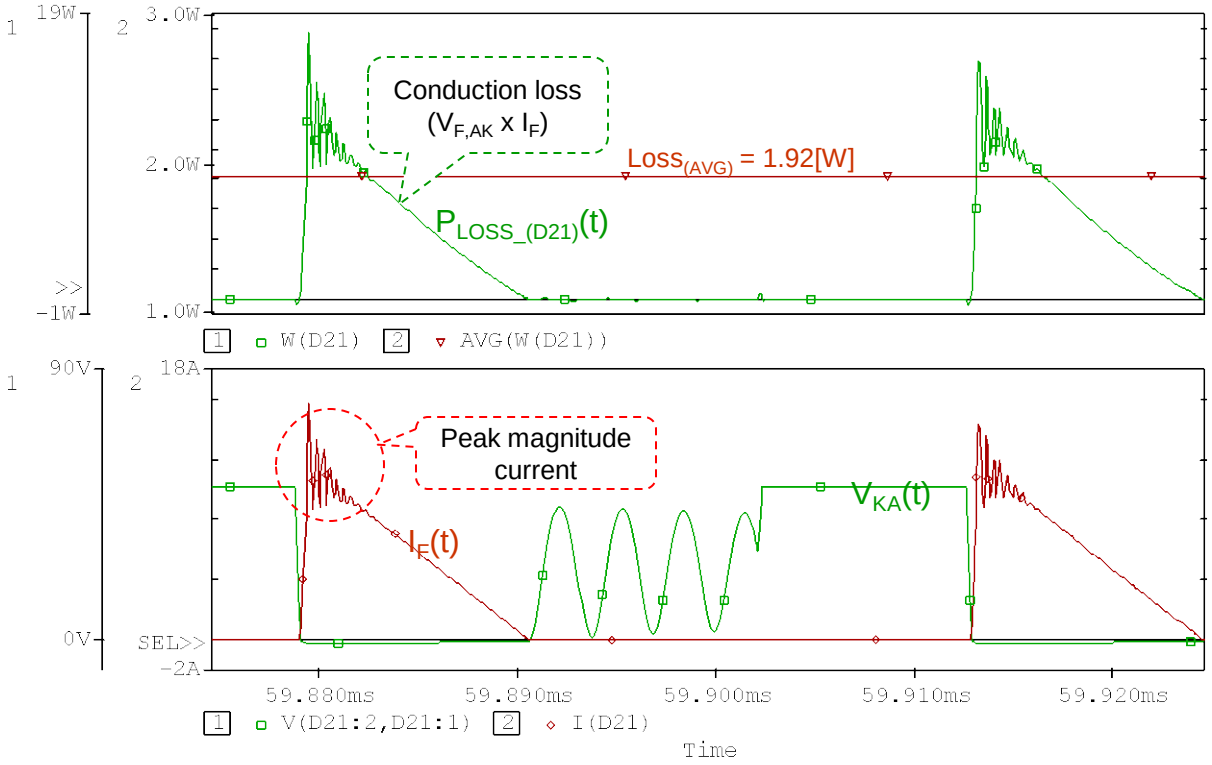
Analysis
Time Domain (Transient)
Run to time: 500ms
Start saving data after: 0
Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation result shows the $V_{KA(D21)}$ peak voltage and the $I_{F(D21)}$ peak current.
- The voltage and current should not exceed the maximum rating of the device D_{21} (SF6L20U : V_{RM}=200V ,I_O=6A ,and I_{OFSM}=80A).

5.2 Losses in D_{21}



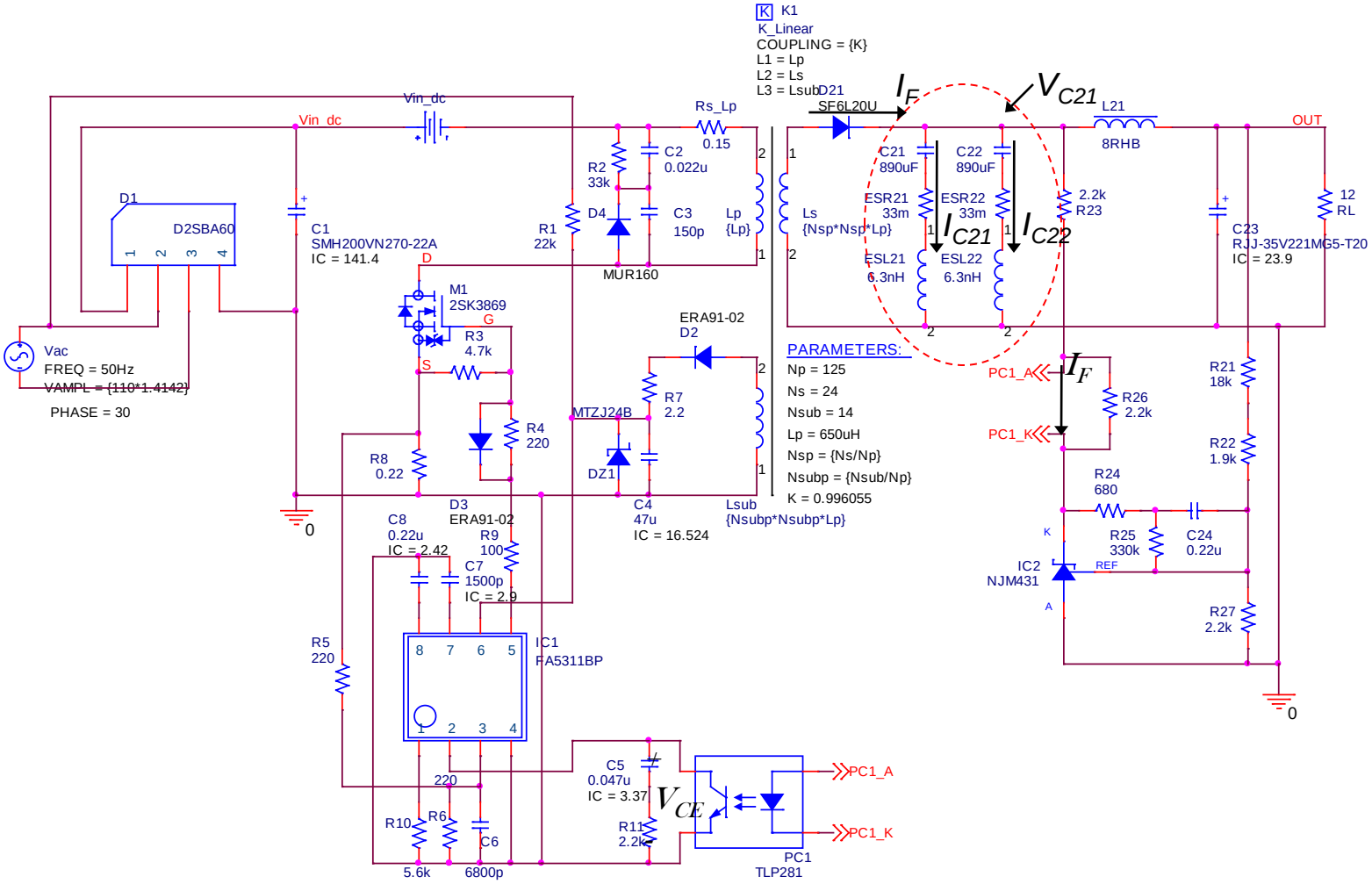
Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation results shows waveforms of I_F and V_{KA} of diode D_{21}. Switching power loss and average power loss are also shown.

6. Output Capacitor C_{21} and C_{22}



6. Output Capacitor C_{21} and C_{22}

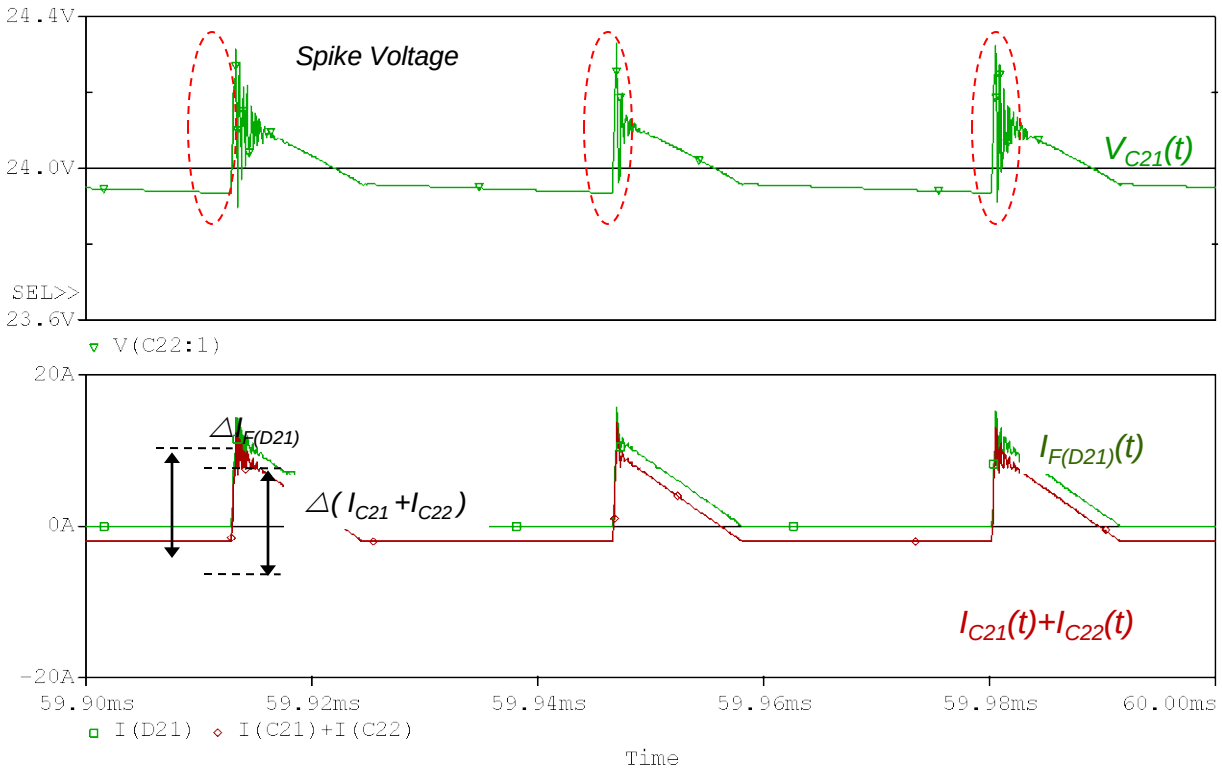
Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation results shows waveforms of $I_{F(D21)}$, I_{C21}+I_{C22} and $V_{C21,RIPPLE}$.
- V_{RIPPLE} is mostly caused by ESR ,that the value is 33mΩ for C_{21} and C_{22}. If the V_{RIPPLE}(240mV) doesn't meet the ripple specification ,additional LC filter stages can be used.

6. Output Capacitor C_{21} and C_{22}



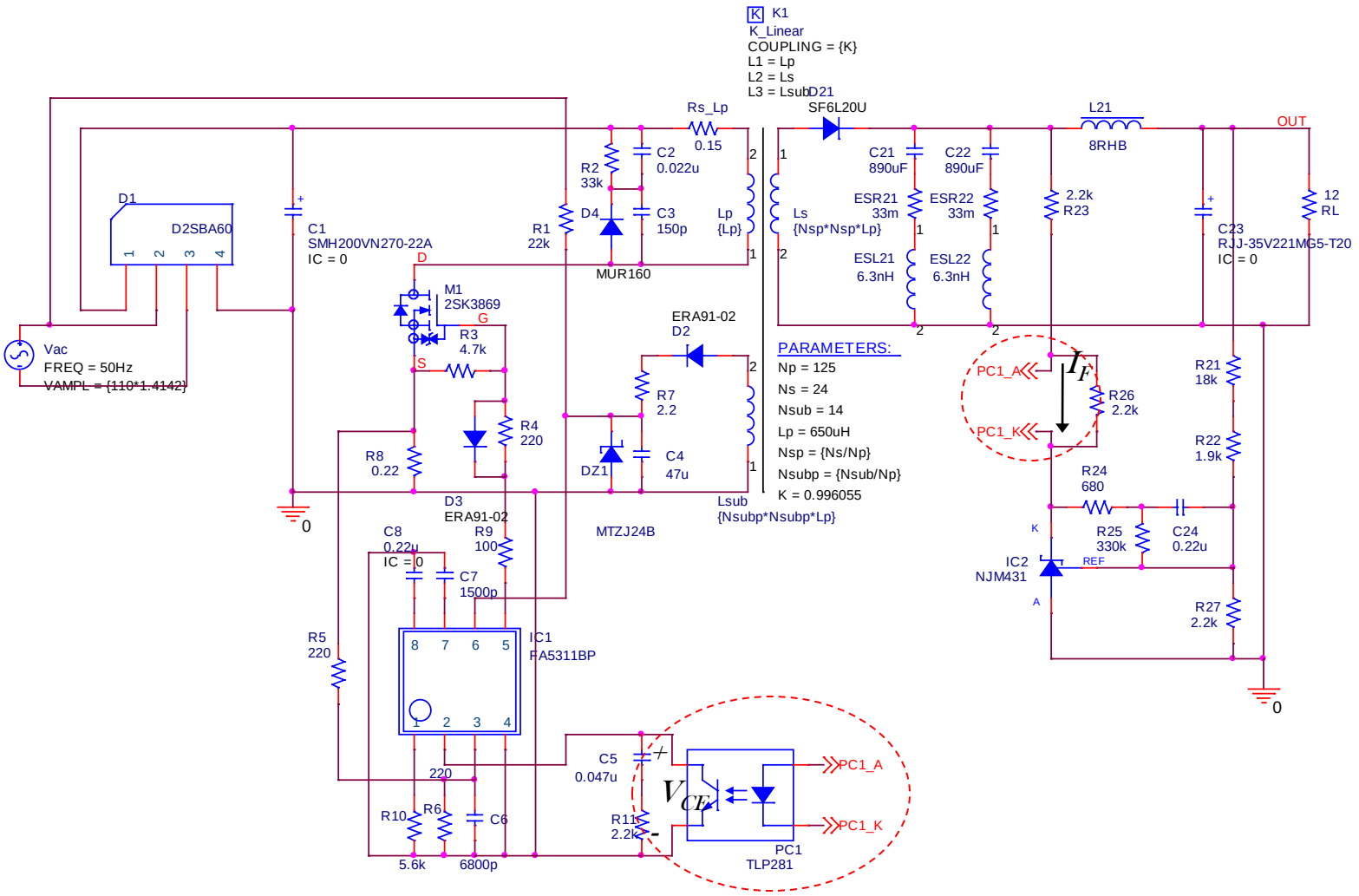
Analysis
Time Domain (Transient)
Run to time: 60ms
Start saving data after: 40ms
Maximum step size: 100ns

.Options

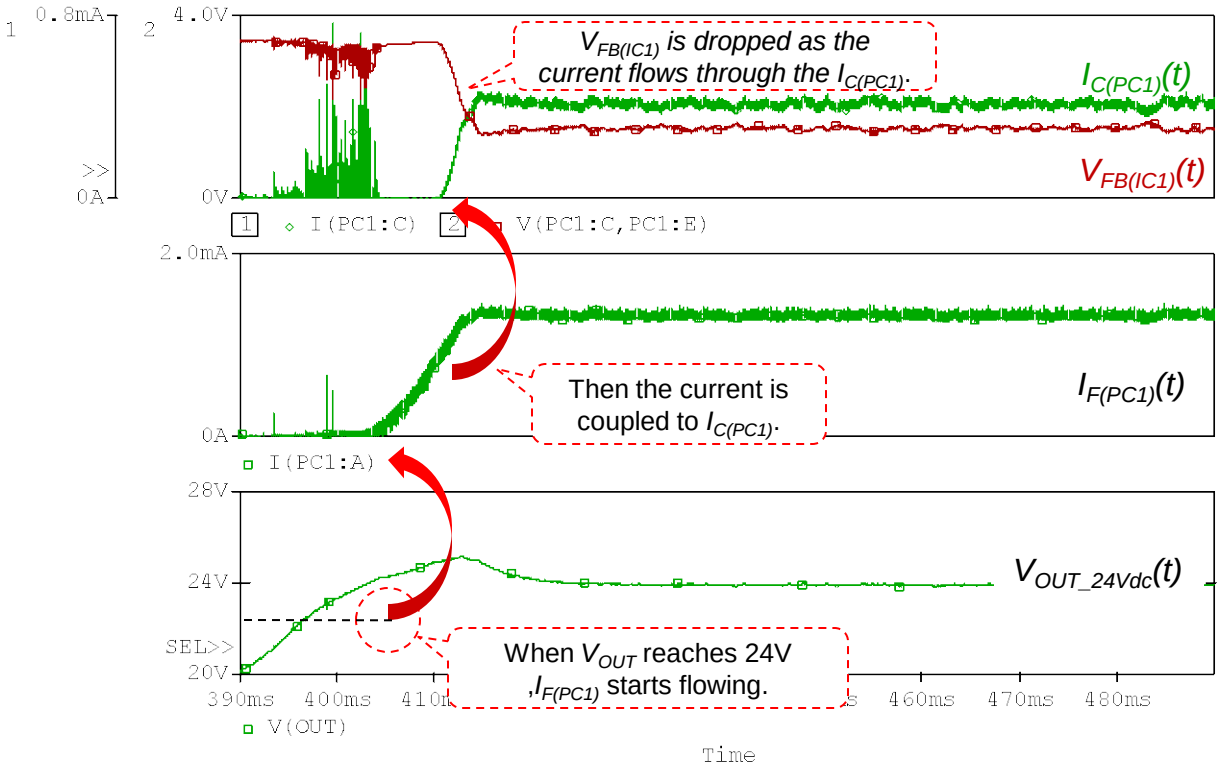
RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- Simulation results shows the spike voltage ,that caused by ESL effect of C_{21} and C_{22}.
- In case the manufacturer doesn't provide this data ,ESR and ESL are measured by Precision Impedance Analyzer.

7. Photocoupler PC_1



7. Photocoupler PC_1



Analysis
Time Domain (Transient)
Run to time: 500ms
Start saving data after: 0
Maximum step size: 10us

.Options

RELTOL:	0.01
VNTOL:	1.0m
ABSTOL:	100.0n
CHGTOL:	0.1p
GMIN:	1.0E-12
ITL1:	500
ITL2:	200
ITL4:	20

- When the power supply output reach the spec voltage (24V), a shunt regulator draws current through photorcouple ($I_{F(PC1)}$).
- Then the current $I_{F(PC1)}$ is coupled to the collector current of the photocoupler $I_{C(PC1)}$. This causes FB pin voltage to decreases ,So the IC can control the output voltage of the power supply.

Simulation Index (1/2)

Simulation Index (2/2)